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DELAY COMPARISON OF BOOTH MULTIPLIER AND VEDIC MULTIPLIER USING VHDL

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ABSTRACT—

Processor's performance is always depends upon its delay. In processors this delay can be reduced by the factor called multiplier. If the delay of the multiplier is reduced then the speed of the processor automatically gets increased. This paper presents design of Booth Multiplier and Vedic multiplier using VHDL (Very High Speed Integrated Circuit Hardware Description Language). Booth multiplier has been designed by using the Booth algorithm concept. Vedic multiplier has been designed by using Vedic mathematics. There are total 16 Sutra's, out of which Urdhva Tirvakbhyam (Vertically and Crosswise) Sutra is used for designing the Vedic multiplier. After designing these two multipliers, delays are compared to know the efficient multiplier. The code is written in VHDL Language and simulation is done in Xilinx 13.1 i.

***Index Terms*—Booth Multiplier, Urdhva Tirvakbhyam, Vedic Mathematics, Vedic Multiplier, VHDL, Xilinx**

Introduction

The main part of processor is ALU (Arithmetic and Logical Unit) and Multiplication is the main function in arithmetic and logical operations. The ancient system of Vedic Mathematics was rediscovered from the Indian Sanskrit texts known as the Vedas, between 1911 and 1918 by Sri Bharati Krisna Tirthaji (1884-1960) from the Atharva Vedas. According to his research all of mathematics is based on sixteen Sutras, or word-formulas. [1]

These formulae describe the way the mind naturally works and are therefore a great help in directing the student to the appropriate method of solution. In the Vedic system difficult problems or huge sums can often be solved immediately by the Vedic method. These striking and beautiful methods are just a part of a complete system of mathematics which is far more systematic than the modern system. Vedic Mathematics manifests the coherent and unified structure of mathematics and the methods are complementary, direct and easy. It's a unique technique of calculations based on simple principles and rules , with which any mathematical problem - be it arithmetic, algebra, geometry trigonometry, or even calculus can be solved mentally. [2]

Hence, Vedic multiplier using Urdhava Tiryagbhyam sutra has less delay and thus they are treated as high speed multipliers as compared to Booth multiplier using the concept of Booth algorithm.

BOOTH MULTIPLIER

The Booth multiplier is a multiplier which takes three bits at a time which reduces the number of partial products in the operation. From these three bits, two bits are from the present pair and the third bit is from the high order bit of an adjacent lower order pair. After examining each triplet of bits, the triplets are converted by Booth logic into a set of five control signals used by the adder cells in the group to control the operations performed by the adder cells. Booth algorithm gives a procedure for multiplying binary integers in signed 2's complement representation on. It operates on the fact that strings of 0's in the multiplier require no addition but just shifting and a string of 1's in the multiplier from bit weight 2_k to weight 2_m can be treated as 2_{K+1}-2_m. [3]

Figure (1) shows the flowchart of Booth algorithm.

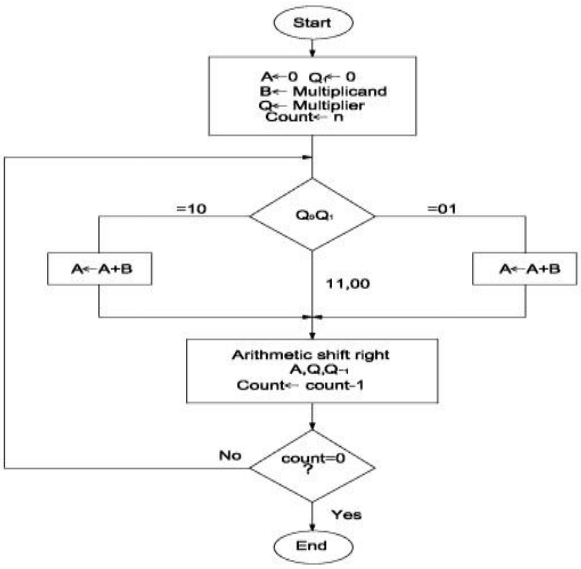

FIGURE 1: FLOW CHART OF BOOTH ALGORITHM [3]

The multiplication of two numbers is carried out such that, the two numbers are represented by a Multiplicand (B) and a Multiplier (Q). Then the conditions are check and operation continues. The operation of Arithmetic Right Shift is performed when the last two digits of the number is 01 0r 10 for each iterations.

Figure (2) shows the multiplication of two numbers using Booth algorithm. It shows multiplication of 5 (0101) with 4 (0100).

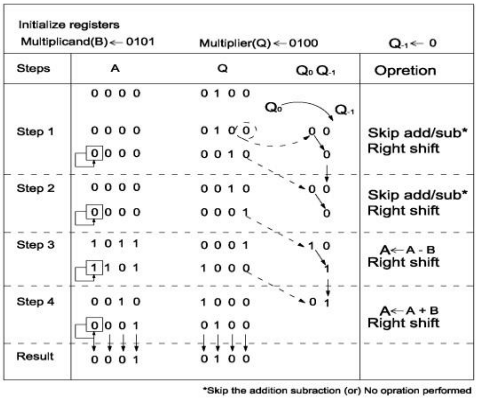

FIGURE 2: EXAMPLE OF BOOTH MULTIPLICATION [3]

Result of the Product 0101 x 0100 is 00010100. From the above example it is proved that the addition or subtraction operation can be skipped if the successive bits in the multiplicand are identical.

VEDIC MULTIPLIER

Vedic mathematics reduces the typical calculations in conventional mathematics to very simple ones. This is so because the Vedic formulae are claimed to be based on the natural principles on which the human mind works. Vedic Mathematics is a methodology of arithmetic rules that allow more efficient speed implementation. UrdhvaTiryakbhyam Sutra is a general multiplication formula applicable to all cases of multiplication. It means "Vertically and Crosswise". The digits on the two ends of the line are multiplied and the result is added with the previous carry. When there are more lines in one step, all the results are added to the previous carry. The least significant digit of the number thus obtained acts as one of the result digits and the rest act as the carry for the next step. Initially the carry is taken to be as zero. [3]

The multiplication using UrdhvaTiryakbhyam Sutra is as follows;

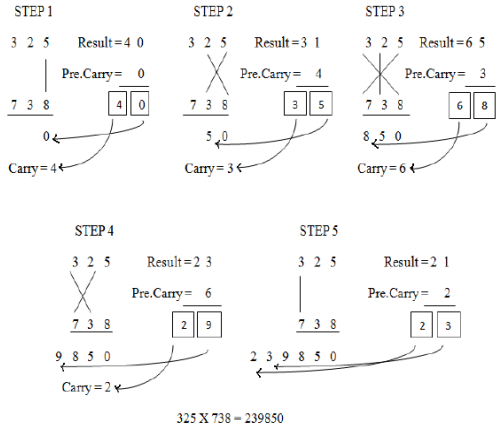

FIGURE 3: MULTIPLICATION OF TWO DECIMAL NUMBERS BY URDHAVA TIRYAKBHYAM SUTRA [4]

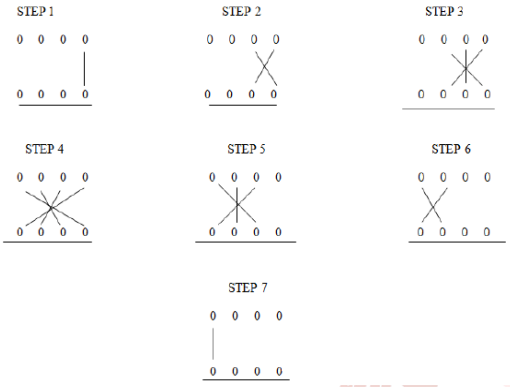

FIGURE 4: LINE DIAGRAM FOR MULTIPLICATION OF TWO 4 – BIT NUMBERS [4]

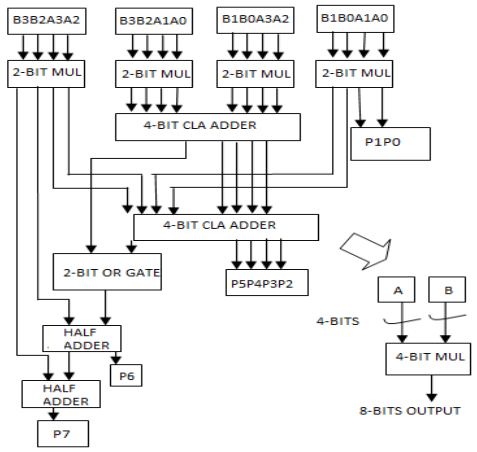

FIGURE 5: 4-BIT MULTIPLIER USING URDHVA TIRYAKBHYAM SUTRA [4]

The design of 4×4 block is a simple an arrangement of 2×2 block. The first step in the design of 4×4 block is grouping the 2 bit of each 4 bit input. These pair terms then form vertical and crosswise product terms. Each input bit-pair is handled by a separate 2×2 Vedic multiplier. The partial products represent the Urdhva vertical and cross product terms. Then using half adder and or assembly the final product will be calculated.

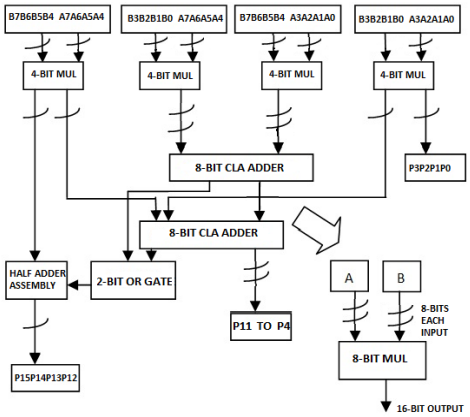

FIGURE 6: 8-BIT MULTIPLIER USING URDHVA TIRYAKBHYAM SUTRA [4]

The design of 8×8 block is a similar arrangement of 4×4 blocks as shown in figure 5. The first step in the design of 8×8 block will be grouping the 4 bit (nibble) of each 8 bit input. These quadruple terms will then form the vertical and crosswise product terms. Each input bit-quadruple is handled by a separate 4×4 Vedic multiplier to produce eight partial product rows. These partial products rows are then added in an 8-bit carry look ahead adder to generate final product bits.

The figure above shows the schematic of an 8×8 block designed using 4×4 blocks. The partial products represent the Urdhva vertical and cross product terms. Then using half adder and or assembly the final product will be calculated.

EXPERIMENTAL RESULTS

RTL SCHEMATIC

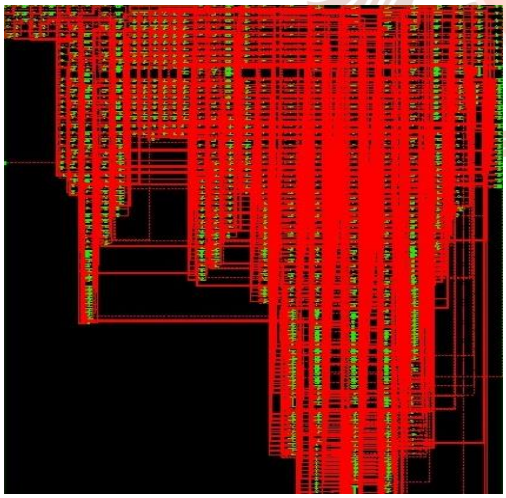

FIGURE 7: RTL SCHEMATIC OF 8BIT BOOTH MULTIPLIER

Figure (7) shows the RTL (Register Transfer Logic) view of Booth Multiplier.

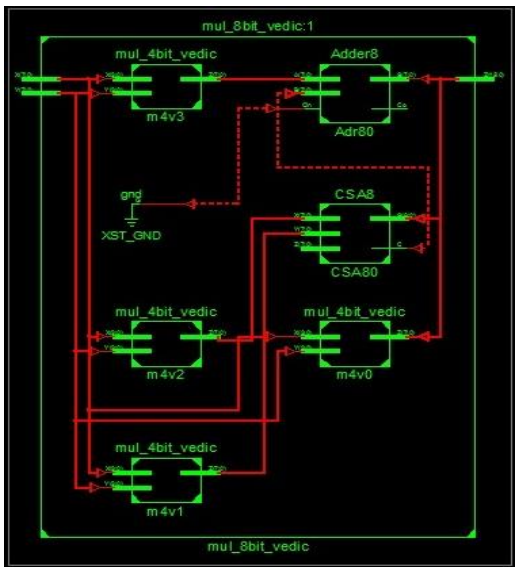

FIGURE 8: RTL SCHEMATIC OF 8BIT VEDIC MULTIPLIER

Figure (8) shows the RTL (Register Transfer Logic) view of Vedic Multiplier.

SIMULATION RESULTS

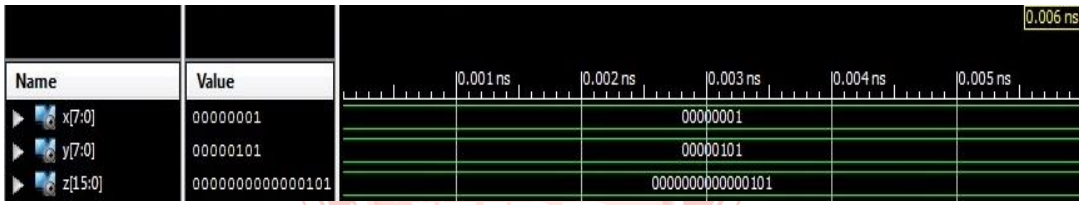

FIGURE 9: SIMULATION RESULT OF 8BIT BOOTH MULTIPLIER

Figure (9) shows the simulation result of 8bit Booth multiplier. Here the two numbers of size 8Bit each representing the variables x and y are multiplied by following the booth algorithm and result will be given by the z variable of size 16Bit.

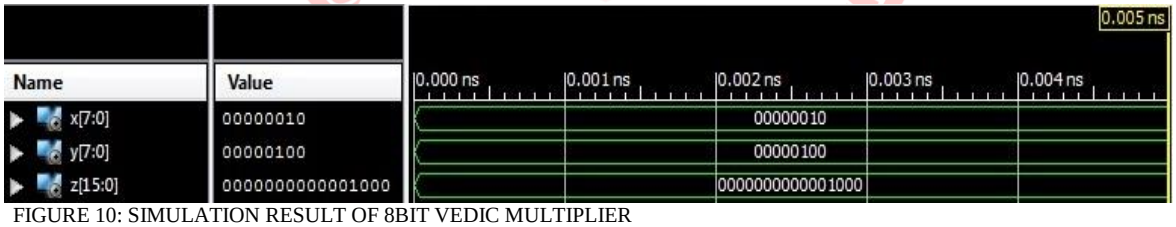

FIGURE 10: SIMULATION RESULT OF 8BIT VEDIC MULTIPLIER

Figure (10) shows the simulation result of 8bit Vedic multiplier. Here the two numbers of size 8Bit each representing the variables x and y are multiplied by following the Urdhava Tiryagbhyam Sutra and result will be given by the z variable of size 16Bit.

Table 1: Delay comparison of Booth and Vedic Multiplier

Delay (in nano seconds)			
VERTEX 6	2x2	4x4	8x8
Booth Multiplier	9.586ns	19.260ns	35.221ns
Vedic Multiplier	7.858ns	17.985ns	32.113ns

CONCLUSION

It can be concluded that Vedic Multiplier is superior in all respect like speed, delay, area, complexity, power consumption. However, Booth multiplier requires more power consumption and gives optimum number of components required, but delay for this multiplier is larger than Vedic Multiplier. Hence, for low power requirement and less delay requirement Vedic multiplier is suggested. Ancient Indian Vedic Mathematics gives efficient algorithms or formulae for multiplication which increase the speed of devices like we use the sutra Urdhva Tiryakbhyam.

The computational path delay is found to be 32.113 ns for 8x8 bit Vedic Multiplier and 35.221 ns for Booth Multiplier. Hence our motivation to reduce delay is finely fulfilled. Hence, we observed that the Vedic Multiplier is much more efficient than Booth Multiplier.

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