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CONVOLUTION AND DECONVOLUTION ALGORITHM USING VEDIC MATHEMATICS FOR HIGH SPEED APPLICATION: A REVIEW

Amit A. Bhutada[1], Prof. Sanjay Tembhurne[2]

[1]G.H.R.A.E.T, Nagpur, [2]G.H.R.A.E.T, Nagpur

[1]ameetbhutada91@gmail.com, [2]sanjay.tembhurne@raisoni.net

ABSTRACT:

Convolution and Deconvolution is having wide area of application in Digital Signal Processing. Convolution helps to estimate the output of a system with arbitrary input, with knowledge of impulse response of the system. Linear systems characteristics are completely specified by the systems impulse response, as governed by the mathematics of convolution. And with the knowledge of impulse response and output of a system we recover the unknown input in deconvolution operation. Convolution and deconvolution is central to many applications of Digital Signal Processing and Image Processing. In Communication for Signal Processing, we use the convolution and deconvolution for a very long sequence is ubiquitous in many application areas. Both operations consume much of time. So our focus to develop more advance and simpler techniques. This paper presents a direct method of computing the discrete linear convolution, circular convolution and deconvolution for high speed. The most significant aspect of the proposed method is the development of a multiplier and divider architecture based on Ancient Indian Vedic Mathematics sutras Urdhvatriyagbhyam and Nikhilam algorithm.

Keywords:

Convolution, Deconvolution, Vedic Mathematics, VHDL

1. INTRODUCTION

A. Convolution:

Convolution is considered to be heart of the digital signal processing. It is the mathematical way of combining two signals to obtain a third signal. Convolution helps to estimate the output of a system with arbitrary input, with knowledge of impulse response of the system. Linear systems characteristics are completely specified by the systems impulse response, as governed by the mathematics of convolution. Convolution is an operation which takes two functions as input, and produces a single function output (much like addition or multiplication of functions).Consider two finite length sequences f(n) and h(n) on which the convolution operation is to be performed with lengths l and m respectively. The output of convolution operation y(n) contains l+m-1 number of samples. The linear convolution off x (n) and h (n) is given by:

$$y(n) = x(n) * h(n) \quad (1)$$

$$y[n] = \sum_{k=-\infty}^{\infty} x(k)h(n-k) \quad (2)$$

B. Deconvolution:

If the impulse response and the output of a system are known, then the procedure to obtain the unknown input is referred to as deconvolution. The concept of deconvolution is also widely used in the techniques of signal processing and image processing. In general, the object of deconvolution is to find the solution of a convolution equation of the form:

$$x * h = y$$

Usually, *y* is some recorded signal, and *x* is some signal that wish to recover, but has been convolved with some other signal *h* before get recorded. The function *h* might represent the transfer function of an instrument or a driving force that was applied to a physical system. If one Know h or at least form of h, then one can perform deterministic deconvolution. If the two sequences x(n) and h (n) are causal, then the convolution sum is

$$y[n] = \sum_{k=0}^{n} x(k)h(n-k)$$

Where

$$x(0) = \frac{y(0)}{h(0)}$$

The fig1. Below shows block diagram of convolution and deconvolution

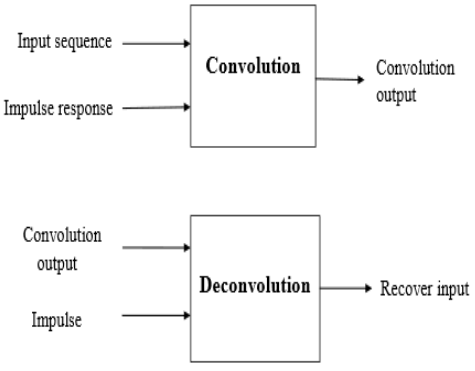

Fig 1: Block Diagram of Convolution and Deconvlution

With continuous advancement in VLSI technology, need of high speed convolution and deconvolution is required. As many areas of Electrical and Electronics Engineering, Digital signal processing plays an important role, discrete convolution and deconvolution is having extreme importance in digital signal processing. Convolution is having wide area of application like designing the digital filter, correlation etc.

So many methods are proposed for performing discrete convolution, one of a tough approach is a graphical method, it is quite sophisticated and systematic but, it is very lengthy and time consuming. The main module for performing convolution and deconvolution is multiplier and divider. Pierre and John have implemented the fast method for performing linear convolution. This method is very easy, it is like to perform simple multiplication of Decimal numbers. And because of this method it is possible to calculate convolution of long sequences very easily. Also a novel method is used for performing deconvolution. This method is similar to calculate long division and polynomial division. As adder is also an important block for the process. The delay and area of all adders is compared. Amongst all adders which having highest speed and occupy less area is used for performing convolution for the conventional multiplication, multipliers with traditional shifts and add method is used. This method is difficult for VLSI implementation and also its delay is too large. Vedic mathematics provides the unique solution for multiplication and division.

Vedic Mathematics, derived from the Veda, provides one line, mental and superfast methods along with quick cross checking systems. Many engineering application areas use this vedic

mathematics, especially in signal processing. It has 16 sutras and sub-sutras which cover all the branches of mathematics such as arithmetic, algebra, geometry, trigonometry, statistics etc. Implementation of these algorithms in processors has found out to be advantageous in terms of reduction in power and area along with considerable increase in speed requirements. These sutras are given in vedas centuries ago. To be specific, these sutras are described in ATHARVA-VEDA. The sutras and sub-sutras were reintroduced to the world by Swami Bharati Krishna Tirthaji Maharaja in the form of book Vedic Mathematics Ancient Indian

2. LITERATURE REVIEW

Surabhi Jain, Sandeep Saini [1] proposed a paper on direct method of computing the discrete linear convolution, circular convolution and deconvolution. The approach is easy to learn because of the similarities to computing the multiplication of two numbers. The most significant aspect of the proposed method is the development of a multiplier and divider architecture based on ancient indian vedic mathematics sutras Urdhvatriyagbhyam and Nikhilam algorithm. The results show that the implementation of linear convolution and circular convolution using Vedic mathematics is efficient in terms of area and speed compared to their implementation using conventional multiplier & divider architectures. According to Mrs.Rashmi Rahul Kulkarni [2], convolution is carried out by serial processing. They used only one 4×4 bit vedic multiplier based on Urdhva Tiryagbhyam sutra. Though hardware is less, delay is more as sixteen multiplications are carried out one by one using only single multiplier. In this paper, convolution of two finite length sequences is computed using direct method. This method is similar to the multiplication of two decimal numbers, this similarity that makes this method easy to learn and quick to compute. As vedic multiplier is high speed multiplier among existing multipliers, Urdhva Tiryagbhyam algorithm from vedic mathematics is used for 4×4 bit multiplication and to improve speed parallel processing approach is used. Similarly Rashmi K. Lomte (Mrs.Rashmi R. Kulkarni), Prof.Bhaskar P.C [3] proposed deconvolution of two finite length sequences (N * M) using direct method to reduce deconvolution processing time. In this paper, they presented an optimized implementation of deconvolution. This particular model has the advantage of being fine-tuned for signal processing. To accurately analyse their proposed system, they have coded there design using the VHDL hardware description language and have synthesized it for FPGA products using ISE. There proposed circuit uses less area and less power. Madhura Tilak, [4] presents a novel method of implementing linear convolution of two proposed method uses modified design approach by replacing the conventional multiplier by vedic multiplier internally in the implementations. There proposed method is efficient in terms of computational speed, hardware resources and area significantly. The efficiency of the proposed algorithm is tested by simulations and comparisons with different design approaches. Dilip J Udhani, Prof. R. C. Patel [5] proposed a new multiplication algorithm which avoids the need of large multipliers by reducing the large number to the smaller number multiplications count which reduces the propagation delay linked with the conventional large multipliers significantly. The structure of the proposed algorithm is based on the Urdhava Tiryagbhyam Sutra (formula) of vedic mathematics which is simply means: “vertical and crosswise

multiplication". The procedure of multiplication using the Urdhava Tiryagbhyam involves minimum calculations, which in turn will lead to reduced number of steps in computation, reducing the space, saving more time for computation. Hence it optimizes to take full advantage of reduction in the number of bits in multiplication. Although Urdhava Tiryagbhyam is applicable to all cases of multiplication, it is more efficient when the numbers involved are large. Ankit Chouhan, Mr. Arvind Pratap Singh [6] presents a paper on high speed vedic multiplier architecture which is quite different from the Conventional vedic multiplier. The most significant aspect of the proposed method is that, the developed multiplier architecture uses carry look ahead adder as a key block for fast addition. Using Carry look ahead adder the performance of multiplier is vastly improved. This also gives chances to break whole design into smaller blocks and use it whenever required. So by using structural modeling they can easily make large design by using small design and thus complexity gets reduced for inputs of larger no of bits.

3. Proposed Work

This paper proposes a systematic design methodology for fast and area efficient digit multiplier based on Vedic Mathematics. In the proposed convolution method the multiplier architecture is based on an algorithm Urdhva Triyagbhyam (Vertical and Crosswise) of ancient indian vedic mathematics. The use of vedic mathematics lies in the fact that it reduces the typical calculations in conventional mathematics to very simple ones. Urdhva Tiryagbhyam Sutra is a general multiplication formula applicable to all cases of multiplication. Urdhva-Tiryakbhyam sutra is first applied to the binary number system and is used to develop digital multiplier architecture. This work presents a systematic design methodology for fast and area efficient digital multiplier based on vedic mathematics. The basic work proposed in this paper is been explained using the block diagram in Fig2.

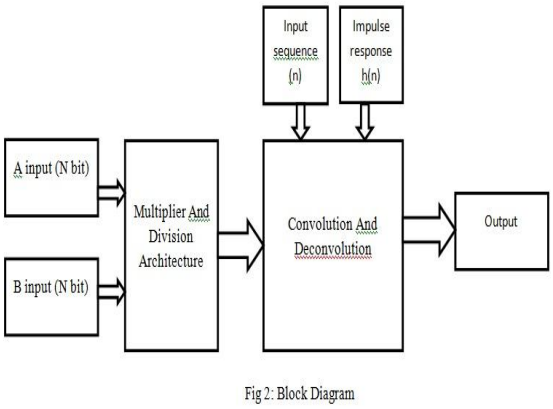

Fig 2: Block Diagram

Vedic Divider: Nikhilam Algorithm literally meaning all from 9 and the last from 10. deconvolution operation is implemented by using nikhilam algorithm based on vedic mathematics while to obtain partial products vedic multiplier is used. The block convolution and deconvolution algorithm is implemented in VHDL (Very High Speed Integrated Circuited Hardware Description Language)

4. REFERENCES

[1] Surabhi Jain, Sandeep Saini," High Speed Convolution and Deconvolution Algorithm (Based on Ancient Indian Vedic Mathematics)" IEEE transaction on January 2014.

[2] Mrs.Rashmi Rahul Kulkarni , (Electronics and Telecommunication, Finolex Academy of Management and Technology/Mumbai

University, INDIA) "Parallel Hardware Implementation of Convolution using Vedic Mathematics"

[3] Lomte, Rashmi K., and P. C. Bhaskar. "High Speed Convolution and Deconvolution Using Urdhva Triyagbhyam." VLSI (ISVLSI), 2011 IEEE Computer Society Annual Symposium on. IEEE, 2011.

[4] Madhura Tilak ,"An Area Efficient, High Speed Novel VHDL Implementation of Linear Convolution of Two Finite Length Sequences Using Vedic Mathematics"

[5] Dilip J Udhani, Prof. R. C. Patel, "Implementation of High Speed Multiplier on FPGA" International Journal of Science, Engineering and Technology Research (IJSETR), Volume 3, Issue 2, February 2014

[6] Ankit Chouhan, Arvind Pratap Singh "Implementation of an Efficient Multiplier based on Vedic Mathematics Using High speed adder" IJISET - International Journal of Innovative Science, Engineering & Technology, Vol. 1 Issue 6, August 2014.

[7] Asmita Haveliya, "FPGA Implementation of a Vedic Convolution Algorithm" ISSN: 2248-9622 www.ijera.com Vol. 2, Issue 1,Jan-Feb 2012, pp.678-684

[8] Rudagi, J. M., Vishwanath Ambli, Vishwanath Munavalli, Ravindra Patil, and Vinaykumar Sajjan." Design and implementation of efficient multiplier using Vedic mathematics." (2011): 162-166.

[9] J. G. Proakis and D. G. Manolakis,"Digital Signal Processing: Principles,Algorithm, and Applications," 2nd Edition. New York Macmillan, 1992.

[10] Pierre, John W."A novel method for calculating the convolution sum of two finite length sequences." Education, IEEE Transactions on 39.1 (1996): 77-80.

[11] Very High Speed Integrated Circuit Hardware Description Language.
URL: http://electrosofts.com/vhdl/.