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LOW-POWER PULSE-TRIGGERED FLIP-FLOP DESIGN WITH CONDITIONAL PULSE-ENHANCEMENT SCHEME

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Abstract

With the growing uses of moveable and wireless electronic systems, reduction in power consumption has become additional and additional necessary in today's VLSI circuits. Over the past decade, power consumption of VLSI chips has perpetually been increasing. Moore's Law drives VLSI technology to continuous will increase in semiconductor unit densities and better clock frequencies. The trends in VLSI technology scaling within the previous couple of years show that the amount of on-chip transistors increase regarding four-hundredth each year. And operation frequency of VLSI systems will increase regarding half-hour each year. though capacitances and provide voltages scale down meantime, power consumption of the VLSI chips is increasing unceasingly.

In CMOS digital circuits, power dissipation consists of dynamic and static parts. Since dynamic power is proportional to the sq. of provide voltage VDD, lowering provide voltage is that the best thanks to scale back power consumptions as long as dynamic power is dominant. With the lowering of provide voltage, semiconductor unit threshold voltage ought to even be scaled so as to satisfy the performance necessities. sadly, such scaling will result in a dramatic increase in leak current, that become a vital concern in low voltage and high performance circuits. For consecutive circuits, there area unit many technologies to scale back their leak power. MTCMOS, leak feedback, gate-length biasing, and DTCMOS are applied in flipflops. MTCMOS technology provides low leak and high performance operation by utilizing high speed and low VT transistors for logic cells and low leak and high VT devices as sleep transistors

INTRODUCTION :

High-Performance flip-flops area unit key parts within the style of latest high-speed integrated circuits. Flip-flops (FFs) area unit the essential storage parts used extensively all told styles of digital styles. specifically, digital styles today typically adopt intensive pipelining techniques and use several FF-rich modules. it's conjointly calculable that the facility consumption of the clock system, that consists of clock distribution networks and storage parts, is as high as 20%–45% of the overall system power. Pulse-triggered FF (P-FF) has been thought-about a well-liked various to the standard master–slave-based FF within the applications of high-speed operations . Besides the speed advantage, its circuit simplicity is additionally useful to lowering the facility consumption of the clock tree system. A P-FF consists of a generator for generating stroboscope signals and a latch for information storage. Since triggering pulses generated on the transition edges of the clock signal area unit terribly slender in pulse dimension, the latch acts like associate degree edge-triggered FF. The circuit complexness of a P-FF is simplified since only 1 latch, as against 2 employed in standard master–slave configuration, is needed.

Despite these blessings, pulse generation electronic equipment needs delicate pulse dimension management to deal with attainable variations in method technology and signal distribution network. A applied math style framework is developed to require these factors into consideration. to get balanced performance among power, delay, and area, style area exploration is additionally a wide used technique. during this temporary, a completely unique low-power P-FF style supported a sign feed-through theme. perceptive the delay discrepancy in latching information "1" and "0," the planning manages to shorten the

longer delay by feeding the signal on to an inside node of the latch style to hurry up the information transition. This mechanism is enforced by introducing a straightforward pass semiconductor unit for further signal driving. once combined with the heartbeat generation electronic equipment, it forms a replacement P-FF style with increased speed and power-delay-product (PDP) performances.

Conventional Explicit Type P-FF Designs:

P-FFs conjointly enable time borrowing across clock cycle boundaries and have a zero or maybe negative setup time. P-FFs area unit so less sensitive to clock disturbance. Despite these blessings, pulse generation electronic equipment needs delicate pulse dimension management within the face of method variation and also the configuration of pulse clock distribution network. looking on the tactic of pulse generation, P-FF styles will be classified as implicit or express. In associate degree implicit-type P-FF, the heartbeat generator may be a intrinsical logic of the latch style, and no express pulse signals area unit generated. In associate degree explicit-type P-FF, the styles of generator and latch area unit separate. Implicit pulse generation is commonly thought-about to be additional power economical than express pulse generation. this is often as a result of the previous simply controls the discharging path whereas the latter must physically generate a pulse train. Implicit-type styles, however, face a prolonged discharging path in latch style, that ends up in inferior temporal order characteristics. the case deteriorates additional once low-power techniques like conditional capture, conditional precharge, conditional discharge, or conditional information mapping area unit applied. As a consequence, the transistors of pulse generation logic area unit typically enlarged to assure that the generated pulses area unit sufficiently wide to trigger the information capturing of the latch. Explicit-type P-FF styles face an analogous pulse dimension management issue, however the matter is additional difficult within the presence of an outsized electrical phenomenon load, e.g., once one generator is shared among many latches.

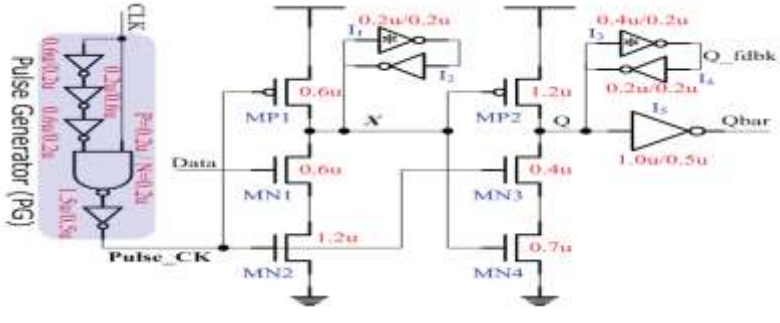

Fig. 1(a): ep-DCO

Fig. 1(b) shows a conditional discharged (CD) technique. An extra nMOS transistor MN3 controlled by the output signal Q_fdbk is employed so that no discharge occurs if the input data remains "1." In addition, the keeper logic for the internal node X is simplified and consists of an inverter plus a pull-up pMOS transistor only.

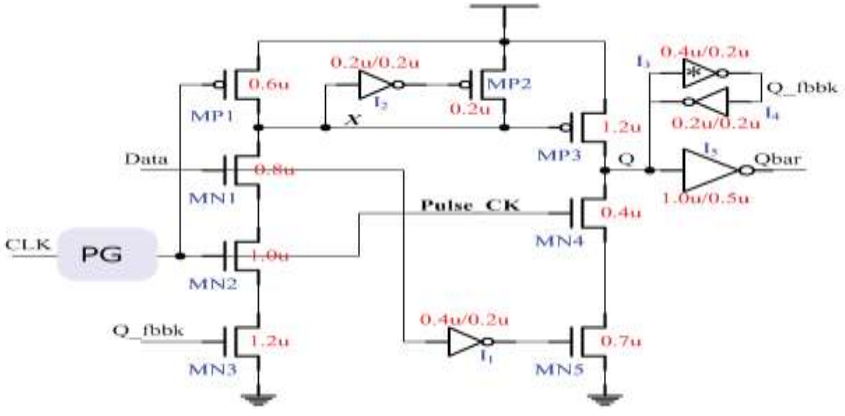

Fig. 1(b): CDFF

Fig. 1(c) shows a similar P-FF design (SCDFF) using a static conditional discharge technique. It differs from the CDFF design in using a static latch structure. Node X is thus exempted from periodical precharges. It exhibits a longer data-to-Q (D-to-Q) delay than the CDFF design. Both designs face a worst case delay caused by a discharging path consisting of three stacked transistors, i.e., MN1–MN3. To overcome this delay for better speed performance, a powerful pull-down circuitry is needed, which causes extra layout area and power consumption.

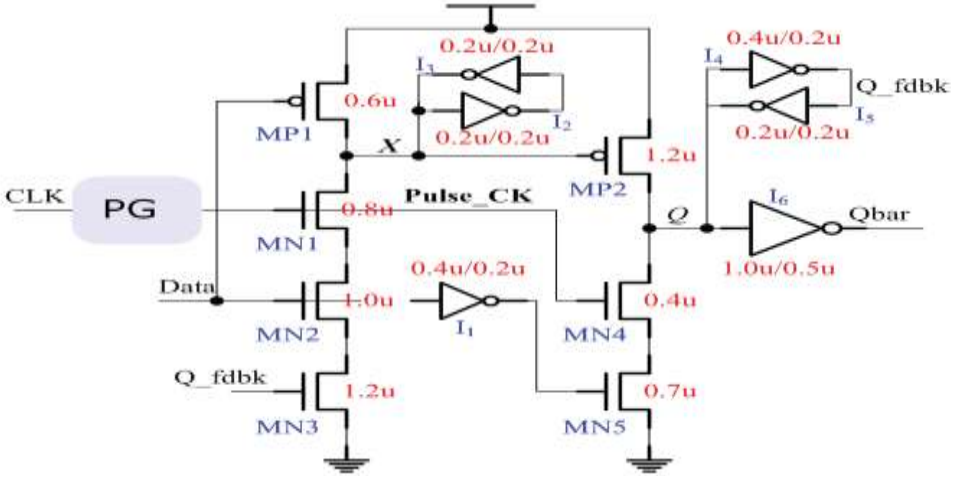

Fig.1(c): Static-CDFF

The modified hybrid latch flipflop (MHLFF) shown in Fig. 1(d) also uses a static latch. The keeper logic at node X is removed. A weak pull-up transistor MP1 controlled by the output signal Q maintains the level of node X when Q equals 0. Despite its circuit simplicity, the MHLFF design encounters two drawbacks. First, since node X is not predischarged, a prolonged 0 to 1 delay is expected. The delay deteriorates further, because a level-degraded clock pulse (deviated by one VT) is applied to the discharging transistor MN3. Second, node X becomes floating in certain cases and its value may drift causing extra dc power.

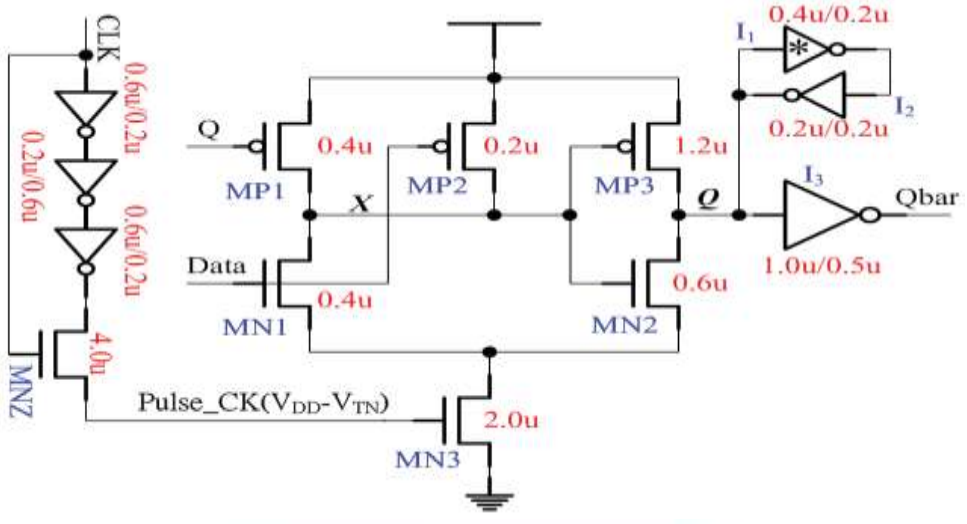

Fig.1 (d): MHLFF

PROPOSED P-FF DESIGN BASED ON A SIGNAL FEED THROUGH SCHEME

To overcome the issues related to the on top of P-FF styles, the subsequent style is introduced that solves the issues of P-FF style still as offer targeted results. the projected style adopts a sign feed-through technique to enhance this delay. like the SCDFF style, the projected style conjointly employs a static latch structure and a conditional discharge theme to avoid superfluous shift at an inside node. However, there area unit 3 major variations that result in a novel TSPC latch structure and create the projected style distinct from the previous one. First, a weak pull-up pMOS semiconductor unit MP1 with gate connected to the bottom is employed within the initial stage of the TSPC latch. this provides rise to a pseudo-nMOS logic vogue style, and also the charge keeper circuit for the interior node X will be saved. In addition to the circuit simplicity, this approach conjointly reduces the load capacitance of node X. Second, a pass semiconductor unit MNx controlled by the heartbeat clock is enclosed so computer file will drive node alphabetic character of the latch directly (the signal feed-through scheme). at the side of the pull-up semiconductor unit MP2 at the second stage electrical converter of the TSPC latch, this further passage facilitates auxiliary signal driving from the input supply to node alphabetic character. The node level will so be quickly force up to shorten the information transition delay. Third, the pull-down network of the second stage electrical converter is totally removed. Instead, the recently used pass semiconductor unit MNx provides a discharging path. The role vie by MNx is so twofold, i.e., providing further driving to node alphabetic character throughout zero to one information transitions, and discharging node alphabetic character throughout "1" to "0" information transitions.

Compared with the latch structure employed in SCDFF style, the circuit savings of the projected style embrace a charge keeper (two inverters), a pull-down network (two nMOS transistors), and an impact electrical converter. the sole further part introduced is associate degree nMOS pass semiconductor unit to support signal feedthrough. This theme really improves the "0" to "1" delay and so reduces the inequality between the increase time and also the fall time delays. In comparison with different P-FF styles like ep-DCO, CDFF, and SCDFF, the projected style shows the foremost balanced delay behaviors. The principles of FF operations of the projected style area unit explained as follows:

When a clock pulse arrives, if no information transition happens, i.e., the computer file and node alphabetic character area unit at a similar level, on current passes through the pass semiconductor unit MNx, that keeps the input stage of the FF from any driving effort. At a similar time, the computer file and also the output feedback Q_fdbk assume complementary signal levels and also the pull-down path of node X is off. Therefore, no signal shift happens in any internal nodes. On the opposite hand, if a "0" to "1" information transition happens, node X is discharged to show on semiconductor unit MP2, that then pulls node alphabetic character high. bearing on Fig. 2(b), this corresponds to the worst case temporal order of the FF operations because the discharging path conducts just for a pulse length. However, with the signal feedthrough theme, a lift will be obtained from the input supply via the pass semiconductor unit MNx and also the delay will be greatly shortened. though this appears to burden the input supply with direct charging/discharging responsibility, that may be a common pitfall of all pass semiconductor unit logic, the situation is completely different during this case as a result of MNx conducts just for a awfully short amount. bearing on Fig. 2(c), once a "1" to "0" information transition happens, semiconductor unit MNx is likewise turned on by the clock pulse and node alphabetic character is discharged by the input stage through this route. in contrast to the case of "0" to "1" information transition, the input supply bearsthe sole discharging responsibility. Since MNx is turned on for less than a brief slot, the loading result to the input supply isn't important. specifically, this discharging doesn't correspond to the crucial path delay and needs no semiconductor unit size tweaking to reinforce the speed. additionally, since a keeper logic is placed at node alphabetic character, the discharging duty of the input supply is raised once the state of the keeper logic is inverted.

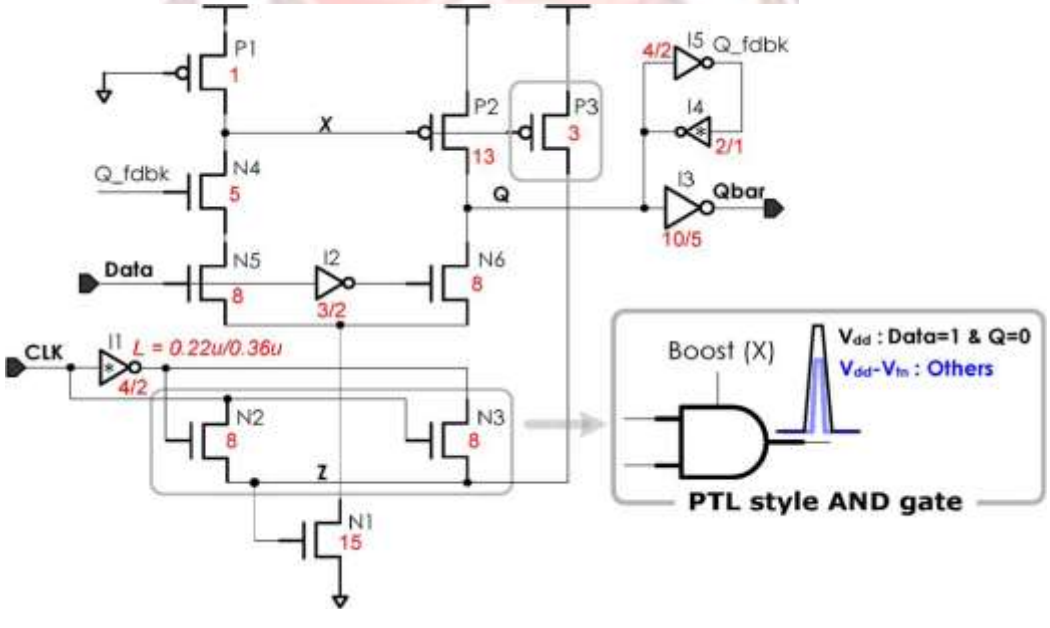

Fig. 2. Schematic of the proposed P-FF design with pulse control scheme.

The projected style, overcome 2 major issues related to existing P-FF styles. the primary one is reducing the amount of nMOS transistors stacked within the discharging path. The other is supporting a mechanism to not absolutely enhance the pull down strength once computer file is "1." In this style, the longest discharging path is made once input data is "1" whereas the Qbar output is "1." to reinforce the discharging under this condition, semiconductor unit P3 is further. semiconductor unit P3 is generally turned off as a result of node is force high most of the time.

JOHNSON COUNTER USING FLIP FLOP DESIGNS

Flip-flops area unit the essential storage parts and might be wont to style registers, counters and memory parts. By planning a Johnson counter victimization such styles, we will prove that the counter designed with pulse sweetening scheme provides low power consumption within the counters.

SIMULATION RESULTS

The design is simulated victimization small wind computer code. the typical power consumed is calculated. the facility consumption varies for various frequencies. For any frequency, the heartbeat sweetening flip-flop shows reduced power consumption compared to different styles. A simulation window seems with inputs and output. the facility consumption is additionally shown on the correct bottom portion of the window.To achieve the target delay, generate the layout once more and run the simulations .Depending on the input sequences assigned at the input, the output is discovered within the simulation

Table.1.Power Consumed By Various Flip-Flops at Different Frequencies

FREQUENCY (Hz)	ip-DCO (MicroWatts)	MHLFF(MicroWatts)	SCCER(MicroWatts)	CPES(MicroWatts)
100 M	649	522	334	85.651
500 M	617	527	336	84.889
1 G	619	535	339	84.427
1.25 G	624	535	340	87.667

2.5 G	641	549	348	92.312
3 G	649	559	350	91.641
5 G	681	587	390	92.011
10 G	743	641	445	113
20 G	52	746	449	139

Table 2: Power Consumed By Johnson Counters at F=2.5 Ghz

FREQUENCY (Hz)	ip-DCO (MicroWatts)	MHLFF(MicroWatts)	SCCER(MicroWatts)	CPES (MicroWatts)
.5 G	2.602	1.824	1.541	0.494

Advantages:

The projected style excels rival styles in performances indexes like power-to-delay and PDP in addition to these styles deserves may be a longer hold time demand inherent in pulse triggered FF styles.

Also the hold time violations area unit abundant easier to mend in circuit style compared with the failure in speed or power

CONCLUSION

In this paper, the assorted Flip-flop styles like, ip-DCO, MHLLF mentioned. The comparison table conjointly further to verify the designed ways. a completely unique low-power pulse-triggered FF style by using 2 new style measures. the primary one with success reduces the amount of transistors stacked on the discharging path by incorporating a PTL-based AND logic. The other supports conditional sweetening to the peak and dimension of the discharging pulse so the dimensions of the transistors within the pulse generation circuit will be unbroken minimum. Simulation results indicate that the projected style excels rival styles in performance indexes like power, _-to-_delay, and PDP. in addition to these style deserves may be a longer hold-time demand inherent in pulse-triggered FF styles. However, hold-time violations area unit abundant easier to mend in circuit style compared with the failures in speed or power.

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