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AN OVERVIEW OF FAULT TOLERANT FIR FILTERS USING ERROR CORRECTING CODES

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Abstract*— Filters are broadly used in dealing out with signal processing and communication systems. The filters so used are digital filters. In those systems, assurance to efficient operation of signal are insignificant and that is why needed implementation of fault tolerant filters. Over the duration, lots of techniques that make use of the filters structure and properties to achieve fault tolerance have been proposed. Enhancing technology make system more complex that include many filters. In those complex systems, it is frequent to have number of filters that functions in parallel. In parallel combination of filters there apply the same filter to different input signals. In recent times, a simple technique having the existence of parallel filters to accomplish fault tolerance has projected. In this brief, that idea is generalized to show that parallel filters can be protected using error correction codes (ECCs) in which each filter is the equivalent of a bit in a traditional ECC. This new scheme allows more efficient protection when the number of parallel filters is large. The technique is evaluated using a case study of parallel infinite impulse response filters showing the effectiveness in terms of protection and implementation cost.

***Keywords*— Error correction codes(ECCs),filters, soft errors.**

INTRODUCTION:

Filters are often used in electronic systems to emphasize signals in certain frequency ranges and reject signals in other frequency ranges. In circuit theory, a filter is an electrical network that alters the amplitude and/or phase characteristics of a signal with respect to frequency. Ideally, a filter will not add new frequencies to the input signal, nor will it change the component frequencies of that signal, but it will change the relative amplitudes of the various frequency components and/or their phase relationships. Today filters are widely used in number of applications which based on automotive, medical, and space where reliability of components in digital electronic circuits is critical. Filters of some sort are essential in the operation of most electronic circuits. There are many different bases of classifying filters and these overlap in many different ways; there is no simple hierarchical classification. As the behavioural properties of signal changes the techniques of filtering it will be differ. Being specific with filter, the digital filters have vast applications in digital signal processing. Filtering is also a class of signal processing, the defining feature of filters being the complete or partial suppression of some aspect of the signal. It is therefore in the interest of anyone involved in electronic circuit design to have the ability to develop filter circuits capable of meeting a given set of specifications. In signal processing, a digital filter is a device or process that removes some unwanted component or feature from a signal. Digital filters are used for two general purposes; separation of signals that have been combined, and restoration of signals that have been distorted in some way. Most often, this means removing some frequencies and not others in order to suppress interfering signals and reduce background noise.

Digital filters are very important part of DSP. In fact, their extraordinary performance is one of the key reasons that DSP has become so popular. As the applications of digital circuits in signal processing reached to its peak, possibilities of faults and its detection and correction within digital circuitry may also need to be advanced. However, filters do not exclusively act in the frequency domain; especially in the field of signal processing many other targets for filtering exist. Correlations can be removed for certain frequency components and not for others without having to act in the frequency domain. It is common in DSP to say that a filter's input and output signals are in the time domain. This is because signals are usually created by sampling at regular intervals of time.

CONCEPT OF FAULT TOLERANCE

A number of techniques can be used to protect a circuit from errors. Those range from modifications in the manufacturing process of the circuits to reduce the number of errors to adding redundancy at the logic or system level to ensure that errors do not affect the system functionality. Digital Filters are one of the most commonly used signal processing circuits and several techniques have been proposed to protect them from errors. There are number of methods used to identify faults and the actions necessary to correct the faults within circuit. Digital filters are widely used in signal processing and communication systems. There are different fault tolerance approaches to conventional computational circuits and the DSP circuits. In some cases, the reliability of those systems is critical, and fault tolerant filter implementations are needed. Over the years, many techniques that exploit the filters structure and properties to achieve fault tolerance have been proposed. In all the techniques mentioned so far, the protection of a single filter is considered.

LITERATURE REVIEW

[1]In this paper, fault tolerance based system based on Error Correction Codes (ECCs) using VHDL is designed, implemented, and tested. It proposes that with the help of ECCs i.e. Error Correction Codes there will be more protected Parallel filter circuit has been possible. The filter they have used for error detection and correction are mainly finite-imulse response (FIR) filters. They have been used Hamming Codes for fault correction in which they takes a block of k bits and produces a block of n bits by adding $n-k$ parity check bits. The parity check bits are XOR combinations of the k data bits. By properly designing those combinations it is possible to detect and correct errors. In this scheme they have used redundant module in which the data and parity check bits are stored and can be recovered later even if there is an error in one of the bits. This is done by re-computing the parity check bits and comparing the results with the values stored. In this way using hamming codes error can be detected and corrected within the circuit.

[2] In this paper, Triple Modular Redundancy (TMR) and Hamming Codes have been used to protect different circuits against Single Event Upsets (SEUs). In this paper, the use of a Novel Hamming approach on FIR Filters is studied and implemented in order to provide low complexity, reduce delay and area efficient protection techniques for higher bits data. A novel Hamming code is proposed in this paper, to increase the efficiency of higher data bits. In this paper, they have proposed technique used to demonstrate, how the lot of overhead due to interspersing the redundancy bits, their subsequent removal, pad to pad delay in the decoder and consumption of

total area of FIR filter for higher bits are reduced. These are based on the novel hamming code implementation in the FIR filter instead of conventional hamming code used to protect FIR filter. In this scheme Hamming code used for transmission of 7-bit data item.

[3] In this paper, the design of a FIR filter with self checking capabilities based on the residue checking is analyzed. Usually the set of residues used to check the consistency of the results of the FIR filter are based of theoretic considerations about the dynamic range available with a chosen set of residues, the arithmetic characteristics of the errors caused by a fault and on the characteristic of the filter implementation. This analysis is often difficult to perform and to obtain acceptable fault coverage the set of chosen residues is overestimated. Obtained result and therefore requires that Instead, in this paper they have showed how using an exhaustive fault injection campaigns allows to efficiently select the best set of residues. Experimental results coming from fault injection campaigns on a 16 taps FIR filter demonstrated that by observing the occurred errors and the detection modules corresponding to different residue has been possible to reduce the number of detection module, while paying a small reduction of the percentage of SEUs that can be detected. Binary logic dominates the hardware implementation of DSP systems

[4] In this paper they have proposed an architecture for the implementation of fault-tolerant computation within a high throughput multirate equalizer for an asymmetrical wireless LAN. The area overhead is minimized by exploiting the algebraic structure of the Modulus Replication Residue Number System (MRRNS). They had demonstrated that for our system the area cost to correct a fault in a single computational channel is 82.7%. Fault tolerance within MRRNS architecture is implemented through the addition of redundant channels. This paper has presented a detailed analysis of the cost of implementing single fault correction capability in a FIR filter using the MRRNS. The fault-tolerant architecture makes use of the algebraic properties of the MRRNS, and has been shown to provide significant area savings when compared with general techniques. This architecture also requires few additional components to be designed, as identical redundant channels are used, and the polynomial mapping stages are simply expanded from the original components.

PROBLEM DEFINITION

The various types of techniques are verified, tested and implemented in digital signal processing circuits having parallel filters as the block to be protected. Digital filters are one of the most commonly used signal processing circuits and several techniques have been proposed to protect them from errors. Most of them have focused on finite-impulse response (FIR) filters. The proposed scheme [1] is based on the application of error correction codes (ECCs) using each of the filter outputs as the equivalent of a bit in and ECC codeword. This is more efficient implementations when the number of parallel filters is large.

As the proposed scheme is more efficient only when the number of filters is large, it limits the area of application to the higher order when implemented using parallel FIR filters. It makes considerable difference in cost when used for lower order application of DSP. Further, the scheme cannot be used to provide more powerful protection using advanced ECCs that can correct failures in multiples

modules. Many properties such as symmetric filters satisfying the perfect reconstruction condition can only be obtained by IIR filters.

OBJECTIVES

There are various objectives over the protection of digital signal processing circuits. The main objectives are given as follows-

1) To achieve fault free digital circuit.

2). To detect and correct errors in digital circuit with more accuracy.

3) To reduce the overhead, required for protection from error.

4) To improve efficiency.

5) To increase the application area from lower to higher order application.

In the proposed work, we are going to extend scheme of IIR parallel filters by using more powerful multibit ECCs i.e. Hamming codes to correct errors on multiple filters.

Proposed Methodology

1) Study of Digital filters and its parallel design over error detection and correction.

2) To study and verify efficiency of previous work using FIR filter response.

3) Designing of IIR filter with same response and different applied input signal.

4) VHDL implementation and verification of parallel IIR filters using Hamming codes.

5) Computing error detection and correction performance.

6) Simulation and performance evaluation.

7) Comparison and study of the results.

CONCLUSION

In this paper a new scheme to protect parallel filters that are commonly found in modern signal processing circuits has presented. The approach is based on applying ECCs to the parallel filters outputs to detect and correct errors. The scheme can be used for parallel filters that have the same response and process different input signals. An objectives has also been discussed to show the effectiveness of the scheme in terms of error correction and problem definition also shows the overheads. The proposed scheme can also make system cost lower. Proposed

work will result in more efficient fault tolerant system using parallel IIR filters based on ECCs, which will meet the goal to achieve low power consumption, increase area of application and high speed.

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