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A REVIEW OF WALLACE TREE MULTIPLIER USING ADIABATIC LOGIC

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ABSTRACT

Wallace Tree Multiplier (WTM) is one of the fastest multiplier used in many data-processing processors to perform fast arithmetic functions. From the structure of the RCWM (Reduced Complexity Wallace Tree Multiplier), it is clear that there is scope for reducing the area and power consumption. This work uses a simple and efficient gate-level modification to significantly reduce the area and power of WTM. Conventional WTM is still area-consuming due to the CMOS switching structure. The logic operations involved in conventional RCWM and WTM are analyzed to study the data dependence and to identify redundant logic operations. RCWM reduced number of half adders used in Standard Wallace Multiplier (SWM) with a slight increase in full adders to reduce the number of gates. Adiabatic Logic eliminated all the redundant logic operations present in conventional RCWM. Experimental analysis shows that this architecture achieves the three folded advantages in terms of area and power.

KEYWORDS : Wallace tree multiplier, adiabatic logic, tanner tool, 8×8 multiplier.

1. INTRODUCTION

Multipliers are one the most important component of many systems. In high speed digital signal processing (DSP) and image processing multiplier play an vital role. In image processing fast Fourier transform (FFT) is one of the most important transform often used. A computational process of fast Fourier transform requires large number of multiplication and addition operation. The execution of these algorithms requires dedicated MAC and Arithmetic and Logic Unit (ALU) architectures. Multipliers and adders are the key element of these arithmetic units as they lie in the critical path. With the recent advances in technology, many researchers have tried to implement increasingly efficient multiplier. They aim at offering low power consumption, high speed and reduced delay.

One such multiplier is Standard Wallace Multiplier (SWM). SWM is fully parallel version of the multiplier, the carry save adders used in SWM are conventional full adders whose carries are not connected, so that three inputs are taken and two words are out. SWM also uses half adders in reduction phase. A Wallace Multiplier is an easily hardware implementable and efficient methodology, that multiplies two integers, proposed by an Australian Computer Scientist Chris Wallace. For unsigned multiplication, up to n shifted copies of the multiplicand are added to form the result. The entire procedure is carried out into three steps: partial product (PP) generation, partial product grouping & reduction, and final addition.

The principle of Wallace tree multiplication. For an n x n multiplication there are n2 partial products that have to be summed. The 1st step in the algorithm involves grouping the partial products into sets of 3. For example, if there are *n'* rows of partial products, 3*[n/3] rows are grouped and the remaining n mod 3 rows are passed to the next stage. Therefore three rows of partial products are grouped together in stage 1, These 3 rows are then sum using full adders and if there are 2 dots in particular column half adders are used. The resulting sum and carry signals from the half and full adders are passed to the next stage. The process is repeated till the entire n partial products are summed. The resulting sum and carry out of the last stage is added using a fast carry propagation adder at the final stage.

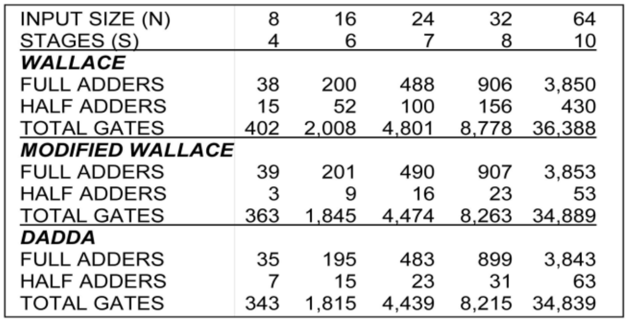
Reduced complexity Wallace multiplier (RCWM) [1] reduced number of half adders used in SWM with a slight increase in full adders to reduce the number of gates. Reduced complexity Wallace Multiplier (RCWM) is the modified version of Standard Wallace Multiplier (SWM). In SWM they use full adder and half adder in their reduction phase, but half adder do not reduced the number of partial bit , therefore RCWM reduced the number of half adder used in the SWM with slightly increase in full adder . The partial products are formed by N**2** AND gates. The partial products are arranged in a Tree structure format. The modified Wallace reduction method divides the matrix into three row groups. Full adders are use for each group of three bits in a column like the Standard Wallace reduction. A two bits group in a column is not processed, so it is passed on to the next stage (in contrast to Standard Wallace method). Single bits are passed on to the next stage as in the Standard Wallace reduction. The only time half adders are used is to ensure that the number of stages does not exceed that of a Standard Wallace multiplier. For some cases, half adders are used in the final stage of reduction. In RCWM they use carry propagating adder (CPA). One possible carry propagating adder for RCWM is a hybrid adder consisting of S+1 ripple carry half adder.

Both the multipliers SWM and RCWM have same number of stages and delay is also same. In Energy Efficient CMOS full adder in reduced complexity Wallace Multiplier at the place of Full adder of standard Wallace Multiplier in order to reduce Area, Power and improvement in speed. An Energy Efficient CMOS Full adder design using alternative logic scheme gives low power delay product (PDP), in terms of speed, power consumption and reduced area. This paper proposes use of new Energy Efficient switching method that is Adiabatic switching for CMOS full adder in reduced complexity Wallace multiplier in order to reduce power even further.

Adiabatic Logic is the term given to low-power electronic circuits. The problem of energy dissipation in smaller and faster circuit is solved by Adiabatic logic. The main causes of energy dissipation in CMOS circuits are due to the charging and discharging of the node capacitor. In adiabatic switching, the process of charging and discharging the node capacitances is carried out in a way so that a small amount of energy is wasted and a recovery of the energy stored on the capacitors is achieved. Adiabatic switching can be achieved by ensuring that the potential across the switching devices is kept arbitrarily small. This can be achieved by charging the capacitor from a time varying voltage source or constant curent source.

2. LITERATURE REVIEW

1. Authors Shahebaj Khan, Sandeep Kakde, Yogesh Suryawanshi proposed a technology entitled "VLSI Implementation of Reduced Complexity Wallace Multiplier Using Energy Efficient CMOS Full Adder" in which modified reduced complexity Wallace Multiplier with reduced power consumption and area by using Energy Efficient CMOS Full Adder at the place of conventional Full adder is presented. From the literature view it can be seen that proposed multiplier reduced power and total number of gate count i.e. area is reduced.

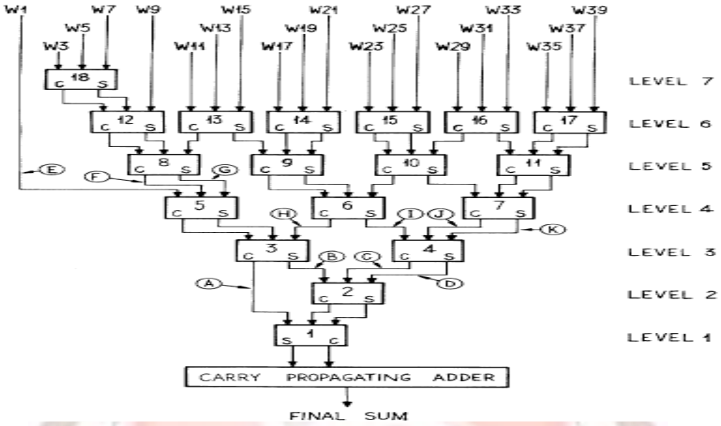


INPUT SIZE (N)	8	16	24	32	64
STAGES (S)	4	6	7	8	10
WALLACE					
FULL ADDERS	38	200	488	906	3,850
HALF ADDERS	15	52	100	156	430
TOTAL GATES	402	2,008	4,801	8,778	36,388
MODIFIED WALLACE					
FULL ADDERS	39	201	490	907	3,853
HALF ADDERS	3	9	16	23	53
TOTAL GATES	363	1,845	4,474	8,263	34,889
DADDA					
FULL ADDERS	35	195	483	899	3,843
HALF ADDERS	7	15	23	31	63
TOTAL GATES	343	1,815	4,439	8,215	34,839

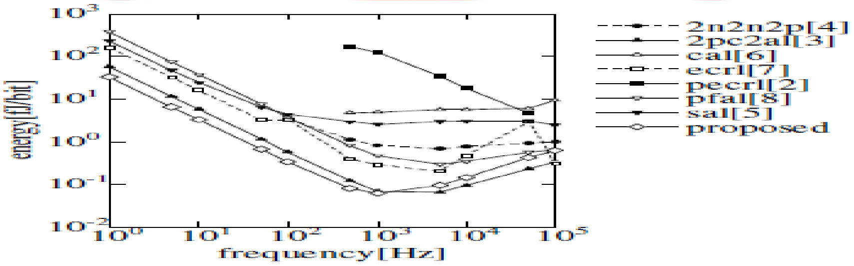
Above table shows the complexity of conventional and modified Wallace reductions as produced with Matlab generator programs. The complexity of Dadda reductions is shown for completeness. The total gate count is based on the use of gate level designs with full adders implemented in nine gates and half adders implemented in four gates. In practice optimized transistor level designs may be used resulting in a different total complexity, but the relative complexity is expected to be generally similar. The table only includes the reductions, neither the N2 AND gates that form bit products nor the carry propagating adder are included. As shown in Table for all word sizes, the modified Wallace reduction uses only a very few full adders which is more than the conventional Wallace reduction. On other hand, the number of half adders is reduced by a factor of five (for the 8-bit reduction) to a factor of eight (for the 64-bit reduction). The total gate count is always less for modified Wallace reduction than the conventional Wallace reduction by 10 (for the 8-bit reduction) to four percent (for the 64-bit reduction). For all word sizes, the modified Wallace reduction uses a few more full adders than the Dadda reduction. The number of half adders is reduced significantly in the modified Wallace reduction. The Dadda reduction requires a slightly smaller total gate count than the modified Wallace reduction, but a complete Dadda multiplier will require more gates due to its larger carry propagating adder. An interesting point is that the sum of the number of full adders and the number of half adders is the same for the modified Wallace reduction and the Dadda reduction. It is not evident why this occurs.

This author presents a modification to the second phase reduction (that reduces N rows of bit products to two rows) used in Wallace multipliers. The modified Wallace reduction reduces the number of half adders required by at least 80 percent compared to the conventional Wallace reduction with only a very slight increase in the number of full adders. Both the conventional Wallace and modified Wallace reductions have the same number of stages and consequently the delay is expected to be the same. It is significant that both the conventional and modified Wallace second phase reductions use more gates than the Dadda reduction, although the penalty is less for the modified Wallace reduction.

2**.** Author C. S. WALLACE suggested a technology for multiplier entitled “A Suggestion for a Fast Multiplier” suggest A Multiplier is an easily hardware implementable and efficient methodology, that multiplies two integers. For unsigned multiplication, up to n shifted copies of the multiplicand are added to form the result. The entire procedure is carried out into three steps 1.partial product (PP) generation 2.partial product grouping & reduction 3.final addition. The following diagram shows the adder tree design by Wallace.



3. Authors Kazunari Kato, Yasuhiro Takahashi, and Toshikazu Sekine in paper entitled “Two Phase Clocking Subthreshold Adiabatic Logic”. They propose a novel sub-threshold adiabatic logic. Our previously proposed ultra low-power subthreshold adiabatic logic has been a problem that noise margin is reduced, so that it is impossible to implement a cascade connection. In this paper, they propose a novel sub-threshold adiabatic logic. To evaluate their proposed circuit, a half adder, full adder, dynamic flip flop and 4×4 array multiplier are designed, and then the operation function and power dissipation are confirmed. From the simulation results, the power dissipation of the proposed multiplier is lower than that of the conventional CMOS.



Above figure shows the comparison of power dissipation of various adiabatic logics and proposed.

To evaluate their proposed circuit, a half adder, full adder, dynamic flip flop and 4×4 array multiplier are designed, and then the operation function and power dissipation are confirmed. From simulation results, the power dissipation of the proposed multiplier is 70% lower than that of the conventional CMOS.

4. Author Nazrul Anuar, Yasuhiro Takahashi, and Toshikazu Sekine in paper entitled “4-bit Ripple Carry Adder using Two Phase Clocked Adiabatic Static CMOS Logic” proposed the low energy operation of 4-bit ripple carry adder (RCA) employing two phase clocked adiabatic static CMOS logic (2PASCL) circuit techniques. They

evaluate NOT, NAND, XOR and NOR logic gates on the basis of the 2PASCL topology using SPICE implemented using 0.18 m CTX CMOS technology. For NOT circuit, the analytical and simulation values are compared. By removing the diode from charging path, the higher output amplitude is achieved and the power consumption of the diode is eliminated. From the simulation results, they noticed that 4-bit 2PASCL RCA can save an average of 71.3% of dissipated energy as compared to that with a static 4-bit CMOS RCA at transition frequencies of 10 to 100 MHz. The results indicate that 2PASCL technology can be advantageously applied to low-power digital devices operated at low frequencies, such as radio-frequency identifications (RFIDs), smart cards, and sensors.

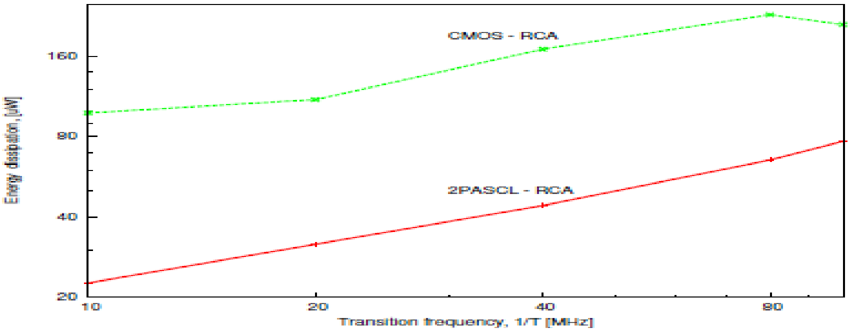
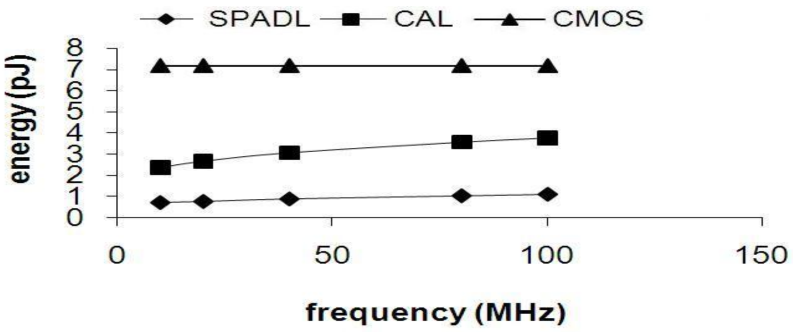


Fig. 11. Output waveforms for 4-bit ripple carry adder (RCA) of 2PASCL from the simulation result (top), and power dissipation of RCAs per cycle over frequency (bottom).

In this paper, they have described the simulation of a 4- bit 2PASCL ripple carry adder (RCA) and its comparison with a CMOS RCA on the basis of adiabatic charging and energy recovery. When the input frequency is 10.100 MHz, the 2PASCL RCA dissipates a minimum of 28.7% of the energy dissipated by a static CMOS RCA. The simulation results show that power consumption in the 2PASCL NOT, NAND, XOR, and NOR circuits are considerably lesser than that in a CMOS. Further, the energy dissipated by a 2PASCL inverter remains low even when the load capacitance is increased. They believe that the proposed adiabatic logic circuits is advantageous for ultra-low-energy computing applications.

5. Authors M. Chanda, A. Dandapat, Toshikazu SekineH. Rahamanin paper entitled “Ultra Low-Power Sequential Circuit Implementation by a Quasi Static Single Phase Adiabatic Dynamic Logic (SPADL)” proposed Implementation of sequential logic circuits by using a novel Quasi-Static Single-phase Adiabatic Dynamic Logic (SPADL) has been presented. SPADL uses only a single sinusoidal source as supply-clock. This not only ensures lower energy dissipation, but also simplifies the clock design which would be otherwise more complicated due to the signal synchronization requirement. Simplicity and static logic resembled characteristics of SPADL logic, substantially decreases circuit complexity with improved driving ability and circuit robustness.

A practical adiabatic asynchronous sequential circuit based on the energy efficient SPADL is implemented with TSMC 0.18µm technology. Spice simulation shows that SPADL 8421 BCD code up counter circuits consume only 30% and 15% energy of single phase Clocked Adiabatic Logic(an existing single-phase based energy recovery logic), and static CMOS at100MHz. Both simulation and measurement results verify the functionality of such logic, making it suitable for implementing energy-aware and performance-efficient sequential circuit.



This authors designed SPADL circuits using single phase ac power supply. Moreover, this paper also explores the design of ultra low-power adiabatic sequential circuits like D, JK, T-flip-flops. Simulation shows that SPADL sequential circuits consume very low energy (only 25%) compared to CAL logic. Although SPADL sequential circuits are used for the design of 8421 BCD code up counter here, other sequential circuit can be realized also.

3. COMPARATIVE STUDY

Table 1. Comparison between Conventional CMOS and Adiabatic circuits.

Designed Circuits	**Technology Used**	**Reduced Power Dissipation in%**
4×4 Array Multiplier	2 Phase Clocking Sub threshold Adiabatic Logic	70
4 bit ripple carry Adder	2 Phase Clocked Adiabatic Static CMOS Logic	71.3
8421 code up counter	Quasi Static Single Phase Adiabatic Dynamic Logic	85
Logic gates	Handshaking Quasi Adiabatic Logic	93
Adiabatic counter	Two Phase Clocked Adiabatic Logic	44

From the comparison of the review papers in above table it is concluded that the circuits implemented by using conventional CMOS technologies have more power dissipation than the Adiabatic logic. The Adiabatic logic design uses different Switching method for CMOS to less power consumption.

4. CONCLUSION

The CMOS Switching method for designing low voltage and low power Wallace Tree Multiplier has been presented. The proposed Adiabatic Switching structure and the RCWM to benefit the high speed and low power. A simple approach is proposed in paper to reduce the area and power of RCWM. This new switching technique offers the great advantage in the reduction of area and also the total power. In this paper, an energy efficient Reduced Complexity Wallace Tree Multiplier Proposed. By the process of charging and discharging the node capacitances is carried out in a way so that a small amount of energy is wasted and a recovery of the energy stored on the capacitors is achieved.. They have analyzed the Adiabatic switching can be achieved by ensuring that the potential across the switching devices is kept arbitrarily small. This can be achieved by charging the capacitor from a time varying voltage source or constant curent source. Due to the small area required for adiabatic switching this multiplier is high speed, low area and very low power multiplier.

5. REFERENCES

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