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DESIGN OF DYNAMIC PARITY BASED ARBITER FOR NoC ROUTER

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ABSTRACT–

NoC means Network on Chip is a new method for communication to solve a problem that challenges system on chip. Network-on-Chip (NoC) is an appealing alternative for communication in SoCs with ability of providing high throughput, low latency and scalability. Using a network to replace global wiring has advantages of structure, performance, and modularity. NoC architecture has two parts: router and data link. The router is a module which can use to store and forward data, and the data link use to transmit signals from one router to its neighbour. And router consist of three part such as input buffer, arbiter, and crossbar. Dynamic priority of a packet is given according to the traffic load of previous router. In certain router, if many packets request the same output channel, the router need to choose one of these packet, and deliver it to next router. In the dynamic priority based round robin arbiter in this they can reduced power consumption and area gate count. The dynamic priority based matrix arbiter and also compare the parameter like area, Power consumption and delay, which we will improve the speed of communication on NoC router. After designing and synthesis of both the arbiter it has been observed that power of matrix arbiter found to be less so Matrix arbiter is more power efficient than Round Robin Arbiter. Along with reduced the number of gate counts ,which can be used to calculate approximated area and also reduction in delay which we will improve the speed of communication on NoC router.

Keywords-Network on Chip (NoC), Dynamic Priority (Dp)

I. INTRODUCTION

Network-On-Chip (NoC) consists of routers, links, and network interfaces. Routers direct data over several links (hops). Topology defines their logical lay-out (connections). Router can store and forward data .Link can transmit signals from one router to its. Network-on-Chip (NoC) is an alternative for communication in SoCs with ability of providing high throughput, low latency and scalability. Network on chip is a communication subsystem on an integrated circuit (commonly call "chip"), typically between IP cores in a system on chip (SoC).Network-On-Chip (NoC) consists of routers, links, and network interfaces. Routers direct data over several links (hops).Network-on-Chip (NoC) is an alternative for communication in

SoCs with ability of providing high throughput, low latency and scalability. NoC architectures are based on packet-switched networks and circuit-switched networks .For circuit-switched networks, routers can be designed with no queuing (buffering).For packet-switched networks, some amount of buffering is needed, to support bursty data transfers. Packet-switched networks has required new and efficient principles for design of routers for NoC.

In recent years, many researches of the NoC design make on effort to improve the performance by using routing algorithm or chaining router architecture Network-On-Chip (NoC) consists of routers, links, and network interfaces. Routers direct researches of the NoC design make on effort to improve the performance data over several links (hops).[1]

II. LITERATURE REVIEW

A. NOC ARCHITECTURE

In the NoC architecture the Network-On-Chip (NoC) consists of links, routers and network interfaces. Routers direct data over several links (hops). Topology defines their logical lay-out (connections). Network-on-Chip (NoC) is an alternative for communication in SoCs with ability of providing high throughput, low atency and scalability..NoC architectures are based on packet-switched networks and circuit-switched networks. A typical NoC consists of computational processing elements (PEs), network interfaces (NIs), and routers.. The NoC architecture has two parts router and data link. The router can store and forward data and the data link can transmit signals from one router to its neighbor.[2]

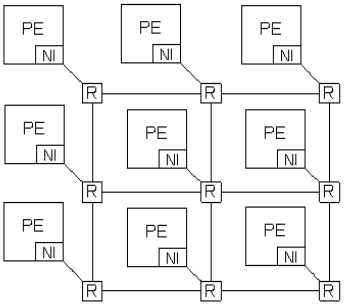

Fig:- Block Diagram of NoC Architecture

This paper proposes the power efficiency of NoC (network on chip) is becoming a new research direction. They had proposed an innovative power-efficient architecture of input buffer of NoC, which makes use of the mentioned characteristics, it can improve the power efficiency of the NoC of tiled CMP significantly. As an important part of a tiled CMP, the NoC architecture is composed with two parts: router and data link. The router is a module which can store and forward data, and the data link can transmit signals from one router to its neighbor. Since the energy consumption of an operation depends on the data of current cycle as well as its continuously previous cycle, They used the data transition as the independent variable for precision. The digital signals transmitted on NoC are occurred by cache coherence protocol . [1]

B. NOC ROUTER ARCHITECTURE

The NoC router architecture consist of three bolck Arbiter, buffer, crossbar. The input buffer stores the input data temporarily, The arbiter receives requests from input buffers and allocates virtual channels to requests and then gives grant signals to request initiators. The crossbar switches granted input requests and forwards the request data to data link, and then the request data is transmitted to the next hop router through data link .In this paper, A NoC Router if more than one input is request for

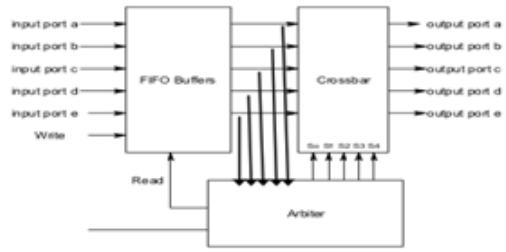

Fig:- Block Diagram of NoC Router

the same output the arbiter is used. Here we are explaining the behavior of Round Robin Arbiter in NoC Architecture. The Round Robin Arbiter operates on the principle that a request which was just served should have a lowest priority on the next round of arbitration. It keeps the updated status of all the ports and knows which ports are free and which ports are communicating with each other. Packets with the same priority and destined for the same output port are scheduled with a Round-Robin Arbiter. In the Round Robin Arbitration scheme, which may be granted that all input request are treated fairly. Hence they had proposed arbiter is suitable for NoC design.[2]

In this paper of design round robin arbiter for NoC architecture. Packets with the same priority and destined for the same output port are scheduled with a round-robin arbiter. Supposing in a given period of time, there was many input ports request the same output or resource, the arbiter is in charge of processing the priorities among many different request inputs. The arbiter will release the output port which is connected to the crossbar once the last packet has finished transmission. After that design the round robin arbiter they analyze the area and power. round robin arbitration scheme, which grantees that all input request are treated fairly .As a result, an arbitration mechanism is necessary to allow only one virtual channel to access a single physical port.[3]

In the paper, Design Matrix Arbiter for NoC architecture .In the matrix arbitration when all input packet have the same priority request for same output port then matrix arbiter generate the matrix depending upon input and this case the destination address is not same so every input port getting a priority so they have to transfer data from source to destination. When all input port are request for same output port in this situation matrix arbiter first form a matrix 5*5. After that matrix arbiter assign the Priority to all input request and generate the grant signal. In this paper analyze the Area, power. In the matrix arbiter the input request is granted according to priority matrix. the round robin arbiter use less resources as compared to matrix arbiter & the matrix arbiter consume more resources because of that it uses maximum clock frequency. [4]

In this paper , For a new packet control circuit is implemented to decide whether the congestion happen and whether the priority scheduler should be used or not. They performed the transmission latency can be reduced with few area overhead. As the NoC demand increased, This method provides a very good solution for heavy traffic loading The method can reduce the transmission latency in uniformly distributed traffic. A priority based method for the output arbiters to eliminate the congestion of NoC. In this transmission latency can be reduced with few area gate count . [5]

III. OBJECTIVE

To develop matrix arbiter with dynamic priority technique to make the arbitration more efficient and independent of deadlocks. Dynamic priority technique to make the arbitration more efficient and to make better communication we will find out Dynamic priority based arbiter for NoC router also contain Low power consumption , delay along with area gate counts.

IV .TOOL USED

Xilinx ISE 13.2i Simulator:-The language used for the coding of arbiter is VHDL in which behavioral and structural style of modeling is used. For simulation and synthesis purpose Xilinx ISE 13.2i version is used. RTL view & synthesis report can be easily obtained in this software. In addition, power calculations can be done using XPower menu in this tool. for the number of gates counts are calculated with help of summery report which is generated after simulation .In this ISE 13.2i the report are generated for different parameter .For calculating delay check the synthesis report which gives the time period of transmitted port.

V . DESIGN OF DYNAMIC PRIORITY BASED ARBITER FOR NOC ROUTER

I. Dynamic Priority Based Round Robin Arbiter

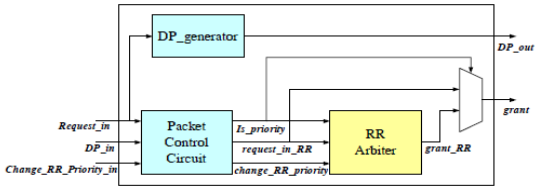

Figure 1:-Block Diagram proposed arbiter architecture for dynamic priority based Round Robin Arbiter

The block diagram of the proposed arbiter architecture. RR Arbiter is the conventional round-robin arbiter and it can be replaced by other arbiter. The DP generator block is used to generate DP. It checks whether the number Request in signal is larger than T . Then generate a signal to the downstream router according to the check result. The Packet Control Circuit block is used to decide which packet can get the output channel. Two priorities are used to schedule the packets. The first is high priority packets. If there is only one packet requests the output, the router will deliver it without arbitration. Otherwise the router arbitrates all the high priority requests by RR scheduling algorithm. While one packet is assigned with high priority, the algorithm will check the priority counter. Once the priority counter is not zero, the counter is increased by one and modulo T . IF all packets are not high priority packet or the priority counter is zero, the router makes a decision according to RR scheduling method and checks the priority counter .Fig. 3.1 shows the block diagram of the proposed arbiter architecture. RR Arbiter is the conventional round-robin arbiter and it can be replaced by other arbiter. The DP generator block is used to generate DP. It checks whether the number Request in signal is larger than T . Then generate a signal to the downstream router according to the check result. The Packet Control Circuit block is used to decide which packet can get the output channel.

II. Dynamic Priority Based Matrix Arbiter

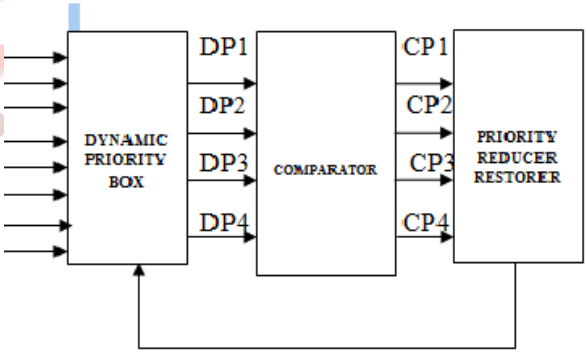

Figure 2 :-Block Diagram proposed arbiter architecture for dynamic priority based Matrix arbiter

The block diagram dynamic priority based matrix arbiter required three main signals First signal is for sending request second signal is for priority and last signal is for to generate grant signal. In the dynamic priority based matrix arbiter sends requests to all 4 priority then it will check the highest priority if the 3 position priority is high

then it will show the grant signal as a 0010 and then it will done up to last position. In the dynamic priority based matrix arbiter the block diagram shows that first block that is dynamic priority box provides dynamic priority it will transfer three signals first is request second is priority and third is grant signal .In the dynamic priority based matrix arbiter sends requests to all 4 priority then it will check the highest priority if the 3 position priority is high then it will show the grant signal as a 0010 and then it will done up to last position. The second block is comparator compares request signal and priority signal it provides CP1 ,CP2, CP3,CP4 it will goes to the next block priority reducer router which gives the priority to enable signal and grant the request signal.

VI . SIMULATION RESULT

In this Simulation Result we studied dynamic priority based Round robin arbiter for NoC router by using scheduler algorithm. Figure .3 shows the Shows the output waveform of dynamic priority based round robin arbiter.

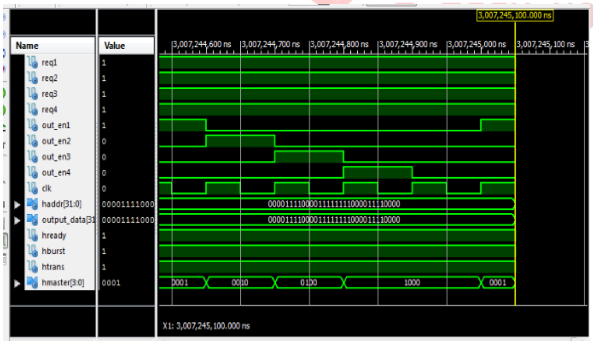

Fig:-3. Output waveform of dynamic priority based Round Robin arbiter

Figure .4. shows the RTL schematic diagram of round robbing algorithm. In this diagram the first signal shows haddress which provides address to the arbiter ,clock pulse is used for sample ,hready is for checking staus ,htrans provides the transfer of data input part tooutput port.

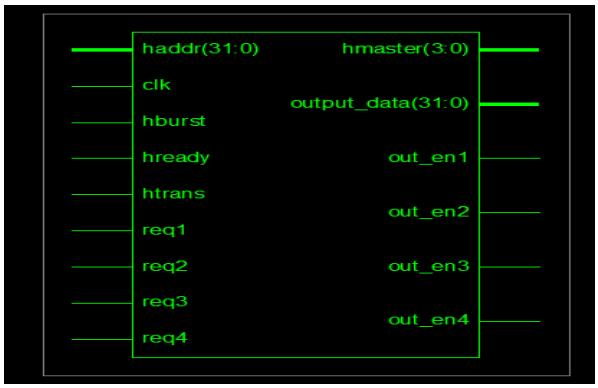

Figure.4:- Schematic Diagram

The Report of XPower is given in table.1 The Total Estimated Power Consumption By dynamic priority based Round Robin Arbiter is 0.46mW

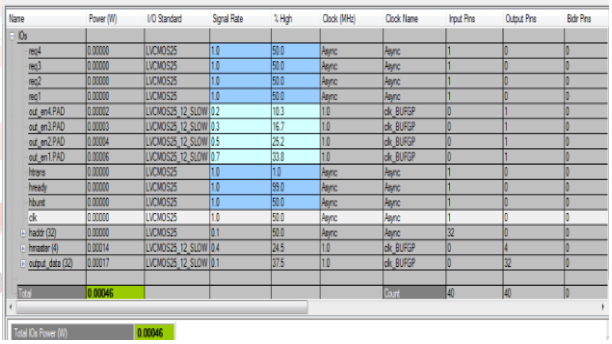

Table.1.Table of total Power Consumption

The Design summery of dynamic priority based Round Robin Arbiter is given in table 2. shows the total equivalent gate count for the design is 127.

Device Utilization Summary				
Logic Utilization	Used	Available	Utilization	Note(s)
Number of Slice Flip Flops	261	29,504	1%	
Number of 4 input LUTs	1,574	29,504	5%	
Number of occupied Slices	837	14,752	5%	
Number of Slices containing only related logic	837	837	100%	
Number of Slices containing unrelated logic	0	837	0%	
Total Number of 4 input LUTs	1,574	29,504	5%	
Number of bonded IOBs	25	250	10%	
Number of BUFGMUXs	1	24	4%	
Average Fanout of Non-Clock Nets	3.69			

Table .2. Table of gate counts

Table 3. shows the synthesis report of dynamic priority based round robin arbiter in which we gaet value of 4.04nsec.

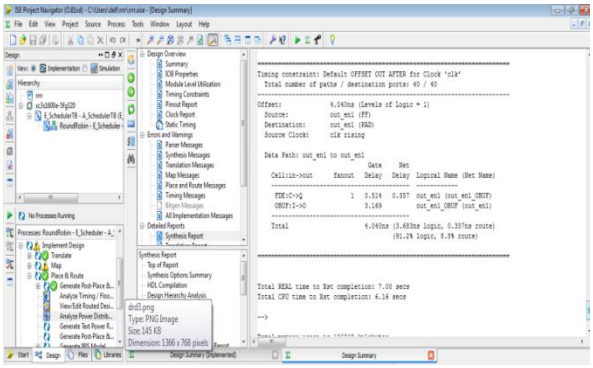

Table 3. Delay

In the Simulation Result we studied dynamic priority based Matrix arbiter for NoC router by using scheduler algorithm. Output waveform of dynamic priority matrix arbiter shows that when all 4 request are enable after particular time interval .Output waveform of dynamic priority based matrix arbiter when for request 1 when output 1 is enable .In the dynamic priority based matrix arbiter shows the output in rotating format

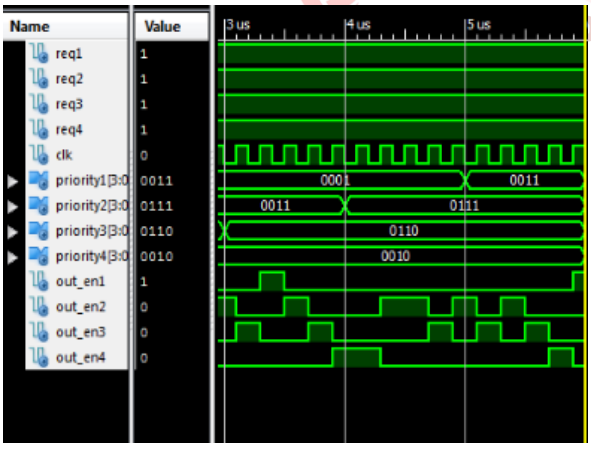

Figure 5:- Output Waveform Of Dynamic Priority Based Matrix Arbiter

Figure 6.:-shows the RTL Schematic Diagram Of Dynamic Priority Based Matrix Arbiter in this arbiter they are four priority signals which provide different priority which is dynamic form.

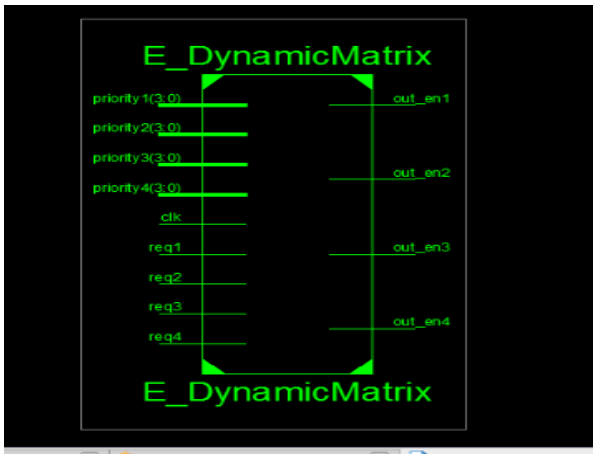

Figure. 6:-Schematic Diagram Of Dynamic Priority Based Matrix Arbiter

The Report of XPower is given in Table.4 The Total Estimated Power Consumption By dynamic priority based Matrix Arbiter is 0.10mW

Table 4. Total Power Consumption

The Design summery of dynamic priority based Matrix Arbiter is given in table 5. Shows the total equivalent gate count for the design is 2650.

Device Utilization Summary				
Logic Utilization	Used	Available	Utilization	Note(s)
Number of Slice Flip Flops	261	29,504	1%	
Number of 4 input LUTs	1,574	29,504	5%	
Number of occupied Slices	837	14,752	5%	
Number of Slices containing only related logic	837	837	100%	
Number of Slices containing unrelated logic	0	837	0%	
Total Number of 4 input LUTs	1,574	29,504	5%	
Number of bonded IOBs	25	250	10%	
Number of BUFGMUXs	1	24	4%	
Average Fanout of Non-Clock Nets	3.69			

Table 5. Table of Gate Counts

Table 6. shows the synthesis report of dynamic priority based matrix arbiter in which wegaet value of 4.04nse

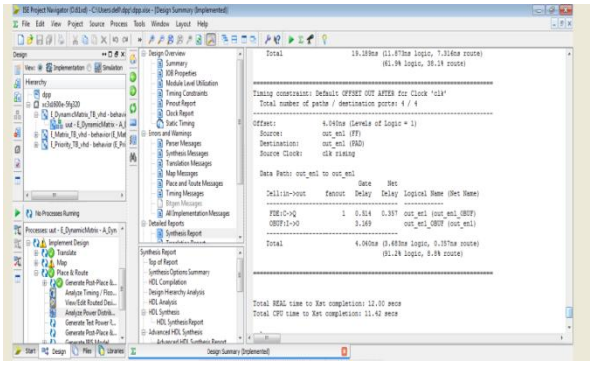

Table 6. Delay

VII. COMPARATIVE STUDY

Comparison for power consumption, gate counts and delay for fixed priority and dynamic priority based round robin arbiter and matrix arbiter in Table 8.

PARAMETER	FIXED PRIORITY (Design & simulation of Round Robin & matrix arbiter)		DYNAMIC PRIORITY (Design of dynamic priority based arbiter)	
	RRA	MA	DPRRA	DPMA
POWER	7mwatt	7mwatt	0.46 mwatt	0.10 mwatt
AREA GATE COUNT	33,489 area gate count	32,352	125 area gate count	2672 area gate count
DELAY	----------	----------	4.04ns	4.04ns

Table 7. Comparative Study

VIII. CONCLUSION

In this paper we studied dynamic priority based Round robin arbiter & matrix arbiter for NoC router by using scheduler algorithm. So, we have designed two arbiter that is dynamic priority based Round Robin Arbiter and Matrix Arbiter. This two arbiter has designed using Xilinx 13.2i tool using VHDL coding. The performance parameter is observed by synthesizing dynamic priority based Round Robin Arbiter for Power, gate counts along with delay by using scheduling algorithm .for Matrix Arbiter observe that the performance parameter the low power consumption , gate count along with delay. a We conclude that performance parameter like power, delay and gate counts by using scheduling algorithm. It is observed that power consumption is reduced for round robin arbiter and matrix arbiter by using dynamic priority as compare to fixed priority. And also reduction in gate counts along with delay .calculate approximate area by using gate counts. Dynamic priority based matrix Arbiter is Power efficient than Round Robin Arbiter The design of dynamic priority based Arbiter for NoC router in which this two arbiter makes more arbitration scheme good for contention and improve the speed of NoC Router.

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