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DESIGN OF 8 X 8 VEDIC MULTIPLIER USING QUATERNARY-LOGIC & PIPELINING ARCHITECTURE

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ABSTRACT—

In recent years the growth of the portable electronic is forcing the designers to optimize the existing design for better performance. There are different entities that one would like to optimize when designing a VLSI circuit. These entities can often not be optimized simultaneously, only improve one entity at the expense of one or more others. A multiplication is the important operation used in various applications like DSP processor, math processor and in various arithmetic circuits. In VLSI system the overall performance is strongly depends on the performance of arithmetic circuits like multiplier. Designers find the solution of these by implementing technique of calculation based on Indian Vedas mathematics called as Vedic multiplier, which offers simple way of multiplication. The design of an efficient multiplier circuit in terms of power, area, and speed simultaneously, has become a very challenging problem. Power dissipation is recognized as a critical parameter in modern VLSI design field. The multi valued logic (MVL) provides the key benefit of a higher density per integration circuit area compared to traditional two valued binary logic. All so the Quaternary logic offers the benefit of easy interfacing to binary logic because radix 4 allow for the use of simple encoding/decoding circuits. This paper present design of 8x8 Vedic multiplier using Tanner EDA tool & simulated using T-spice simulator. With the help of pipelining technique 8x8 Vedic multiplier circuit level has been proposed in these paper, as it does not increase the hardware that much, but which increase the speed and requires less computation gives us better speed. The two stages pipelining is used to optimize Delay compared with previously normal 8x8 Vedic multiplier results.

Index Terms— **VLSI, Multi-valued logic (MVL), Quaternary logic, Vedic multiplier, Digital signals processing.**

INTRODUCTION

A multiplier is one of the most important parts in any processor and most of the instruction in a typical processor is multiplication. Multiplication process is used in many neural computing and DSP applications like Instrumentation and

Measurement, Communications, and Audio and Video processing, Graphics, Image Enhancement, 3-D Rendering, Navigation, Radar, GPS, and control applications like Robotics, Machine Vision and Guidance. In binary logic, the size of the device is reduced by reducing the size of the transistor. But up to a limit, because the size of transistor cannot be reduced indefinitely. The multi-valued logic apply to the multiplier design, word length & no of transistor can be greatly reduced. There are various multipliers for binary logic Such as Array multiplier, Booth multiplier, and Wallace tree multiplier and a Vedic multiplier. In recent years Vedic multiplier has caught the Attention because of its superiority over other multipliers. If the Functional blocks designed in multi-valued logic are used in Vedic multiplier's architecture, it will surely enhance the performance of multiplier and hence the whole area & power consumption of chip. The performance of two levels binary logic is limited due to interconnects which occupy a large area on a VLSI chip. In VLSI circuit, total 70% of the area is divided to interconnection, 20% to insulation, and 10% to device. One can achieve a cost-effective way of utilizing Interconnections by using a larger set of signals over the same area in multiple-Valued logic (MVL) devices, allowing easy implementation of circuits. In MVL advantage of binary logic is retained. The higher radix in Use is the ternary and the quaternary logic. The Binary logic has many drawbacks and limitations. A signal cannot always be just ON or OFF or DON'T CARE, and HIGH IMPEDANCE. It does not mean that these states can result in inefficient processing of the data. Also, binary logic results in longer word-lengths which increase the number of interconnections and hence the chip size. Multiplier design in Vedic mathematics has improved conventional delay time, area size to minimizing power dissipation while still maintaining the high performance. The low power and high speed multipliers can be implemented with different logic style.

VEDIC MATHEMATICS

A 'Veda' is a Sanskrit word that means 'knowledge'. The name Vedic Mathematics which is used & heard many times with reference to the techniques for solving problems mentally. The techniques of math that is Vedic mathematics were rediscovered in the early twentieth century from ancient Indian sculptures by Sri Bharati Krishna Tirthaji Maharaj. These methods can be directly applied to Trigonometry, plain & spherical geometry, conics, calculus and applied mathematics of various kinds. Total 16 sutras or formulae given in ancient Vedas out of these two sutras are useful for multiplication namely Nikhilam sutra and Urdhva Tiryakbhyam sutra. Means "all from 9 and last from 10" and "vertically and crosswise". The Urdhava Tiryakbhyam sutra is more popular than Nikhilam sutra since it is applicable in all cases.

III. MULTI-VALUE LOGIC (MVL)

It was first proposed by Jan Lukasiewicz, Polish minister of Education in 1919. Followed by Emil Post**,** American logician born in Poland the MVL employs more than two discrete levels of a signal, such as ternary & quaternary logic. Two logic systems are available in ternary logic, balanced ternary logic -1, 0 and 1 and simple ternary logic 0, 1 and 2. The quaternary logic uses 0, 1, 2 and 3 logic levels.

IV. OPERATING MODE OF MVL

MVL can be employed in either Voltage-Mode or Current-Mode. In voltage-mode MVL, operating voltage range is divided into the number of logical

values to be represented, whereas, in current-mode MVL, currents are usually defined to have logical levels that are integer multiples of a reference current unit. For higher radix MVL system, current-mode is always preferred over voltage-mode because currents can be copied, scaled and algebraically sign-changed with a simple current mirror. The frequently used linear sum operation can be performed simply by wiring, resulting in a reduced number of active devices in the circuit. It is believed that current-mode MVL designs can allow better noise margin than voltage-mode MVL designs.

V. URDHVA-TIRYAKBHYAM SUTRA

Urdhva Tiryakbhyam Sutra is a general multiplication formula applicable to all cases of multiplication. It literally means "Vertically and crosswise". It is based on a novel concept through which the generation of all partial products can be done and then, concurrent addition of these partial products can be done. Thus parallelism in generation of partial products and their summation is obtained. The Urdhva Tiryakbhyam sutra (method) was selected for implementation since it is applicable to all cases of multiplication. Multiplication of two no's using Urdhva Tiryakbhyam sutra is performed by vertically and crosswise, crosswise means diagonal multiplication and vertically means straight above multiplication and taking their sum. Thus any multi-bit multiplication can be reduced down to single bit multiplication and addition using this method. Moreover, the carry propagation from LSB to MSB is reduced due to one step generation of partial product.

VI. CONCEPT OF PIPELINING

Pipelining is one of the popular methods to realize high performance computing platform. Pipelining is a technique where multiple instruction executions are overlapped. It comes from the idea of a water pipe continue sending water without waiting the water in the pipe to be out. By pipelining the unit of a system we can produce result in every clock cycle. It leads to a reduction in the critical path. It can either increase the clock speed (or sampling speed) or reduces the power consumption at same speed in a system.

VII. MULTIPLIER

A multiplier is an essential component. Longer word-lengths in binary logic make the multiplier large and complex. In binary logic, the size of the device is reduced by reducing the sizes of the transistors. But it has a limit, since the sizes of transistors cannot be reduced indefinitely. By applying MVL to the multiplier design, word-lengths and the area can be reduced. This will enhance the performance of multipliers and hence the whole chip.

A. 2X2 Vedic Multiplier

In 2x2 bit multiplier, the multiplicand has 2 bits each and the result of multiplication is of 4 bits. So in input the range of inputs goes from (00) to (11), output lies in the set of (0000, 0001, 0010, 0011, 0100, 0110, 1001). By using Urdhva Tiryakbhyam, the multiplication takes place. Here multiplicands a And b are taken to be (10) both. The first step is the vertical multiplication of LSB of both multiplicands, and second step is the crosswise multiplication and addition of the partial products. Then Step 3 involves vertical multiplication of MSB of the multiplicands and addition with the carry propagated from Step 2.

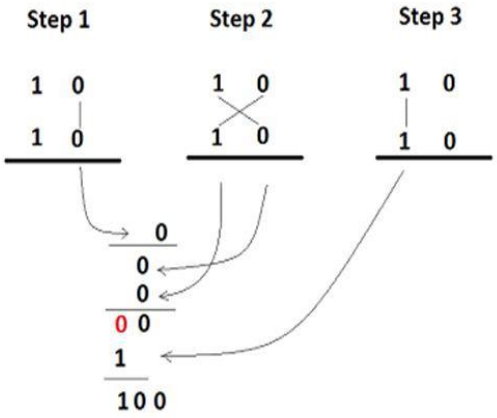
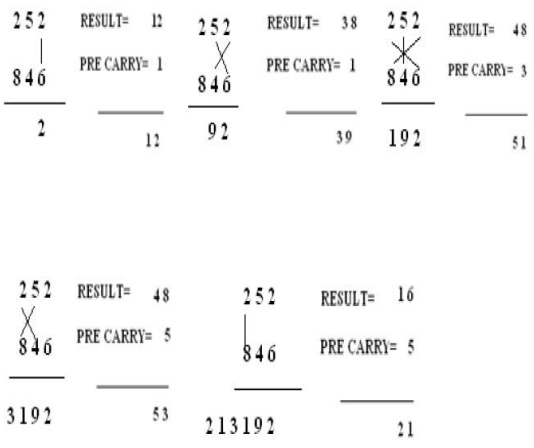


Fig 1: 2X2 Multiplication using Urdhva Tiryakbhyam Sutra.

B. Multiplication of two Decimal Numbers 252 x 846.

For Example, let us consider the multiplication of two decimal numbers 252 x 846 by Urdhva-Tiryakbhyam method. The digits on the both sides of the line are multiplied and added with the carry from the previous step. This generates one of the bits of the result and a carry. This carry is added in the next step and hence the process goes on. If more than one line are there in one step, all the results are added to the previous carry. In each step, least significant bit acts as the result bit and all other bits act as carry for the next step. Initially the carry is taken to be zero.



C. 4X4 Vedic Multiplier

The block diagram of 4x4 Vedic Multiplier is shown in Figure2. This multiplier is modelled using structural style of modelling using VHDL. In this paper first a 2x2 Vedic Multiplier is implemented using the above mentioned method. The 4x4Vedic Multiplier is designed. Using four 2x2 Vedic Multipliers After that 8x8 Vedic Multiplier is implemented using four 4x4 Vedic Multipliers by using pipeline concept. Finally the results will be compared with the standard results.

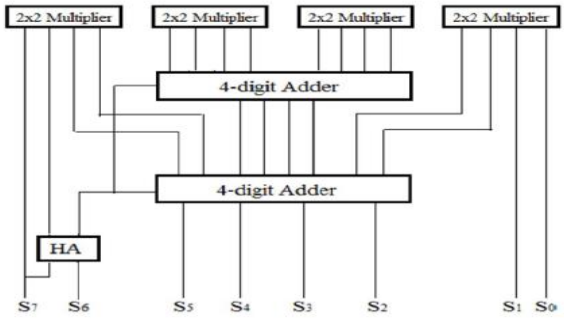


Fig 2:- Quaternary 4x4 Vedic Multiplier.

VIII. Simulation & Results

Fig.3 shows Four Quadrant Vedic multiplier. It can be surely concluded that the Application of current-mode MVL reduces the number of adders in the multiplier architecture as the number of bits to be processed goes on increasing. Furthermore, proposed 4×4 quaternary multiplier and by using pipeline architecture design of 8×8 Vedic Multiplier, which shows great reduction in the circuitry because of MVL.

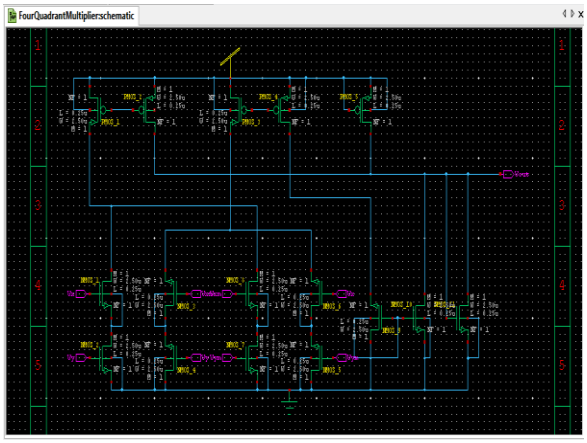


Fig.3. Synthesize result of Four Quadrant Vedic Multiplier.

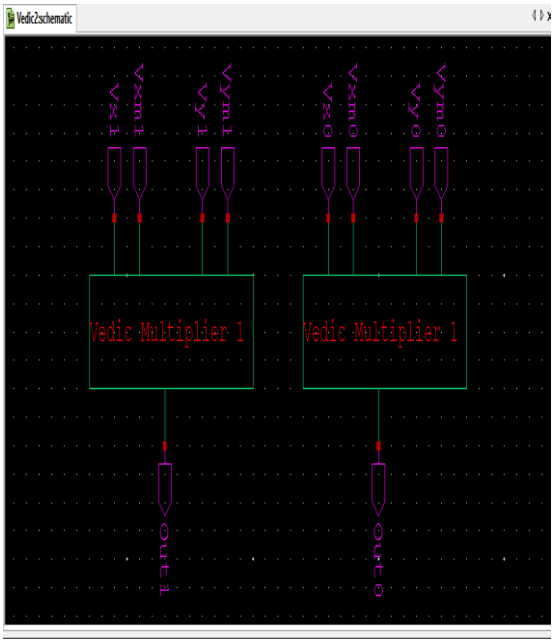


Fig 5:- 2-Sample/Bit Vedic Multiplier

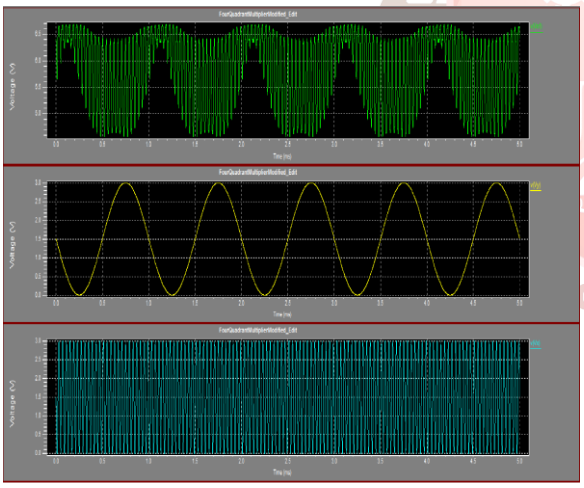


Fig.4. Simulation result of Four Quadrant Vedic Multiplier.

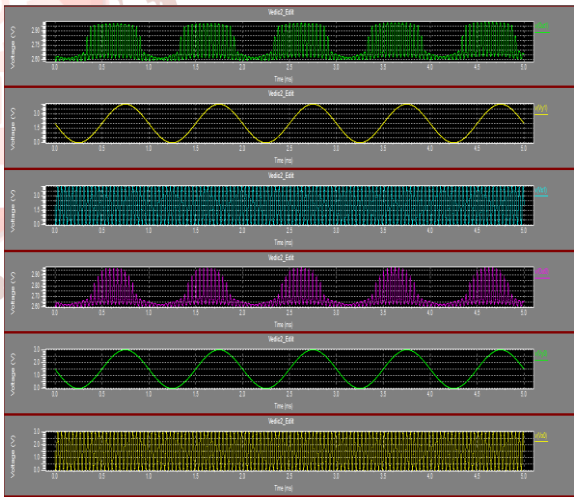


Fig.6:-Simulation result of 2-Bit Vedic Multiplier

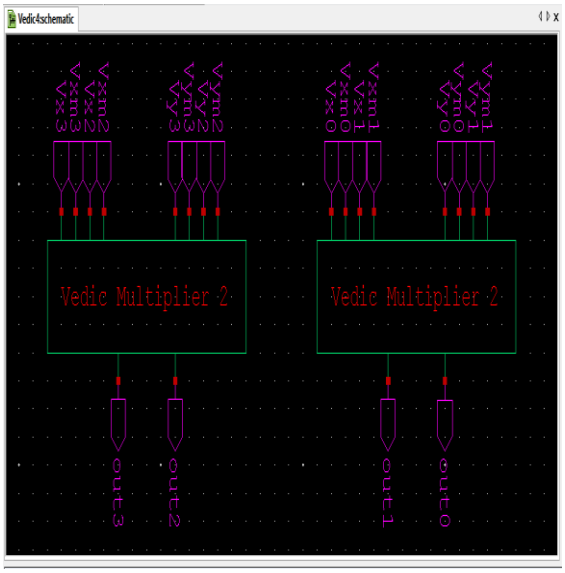


Fig 7:- 4-Sample/Bit Vedic Multiplier

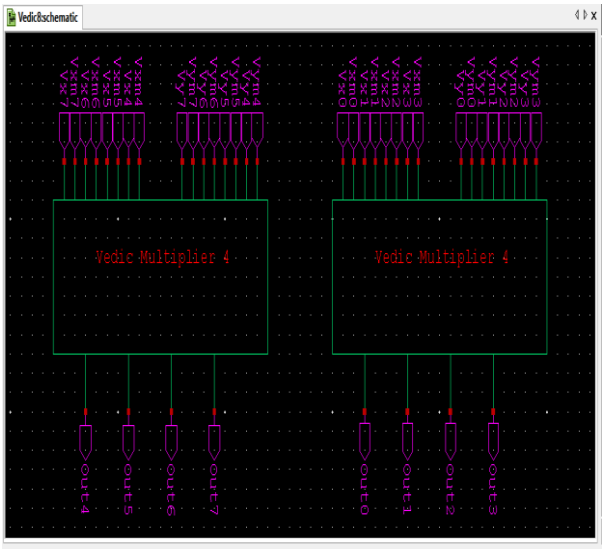


Fig 9:- 8-Sample/Bit Vedic Multiplier

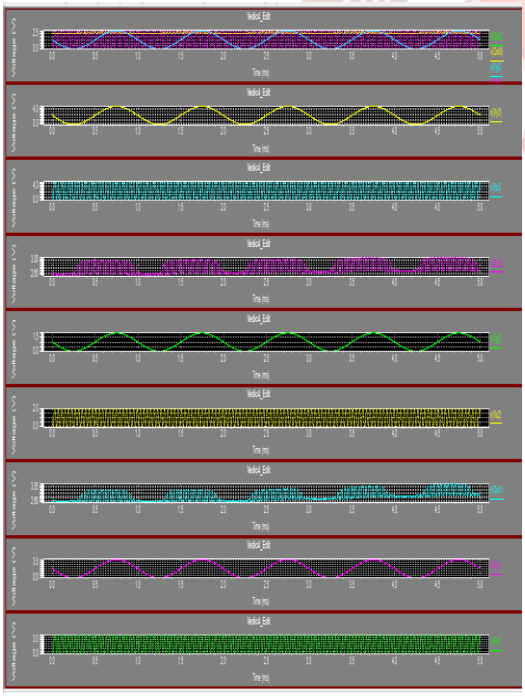


Fig.8:-Simulation result of 4-Bit Vedic Multiplier

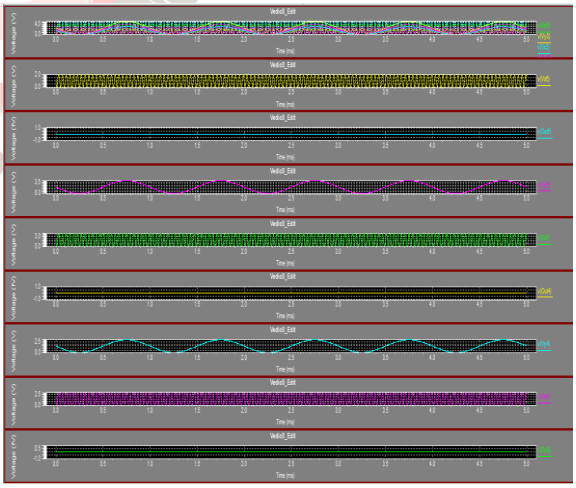


Fig. 10:-Simulation result of 8-Bit Vedic Multiplier

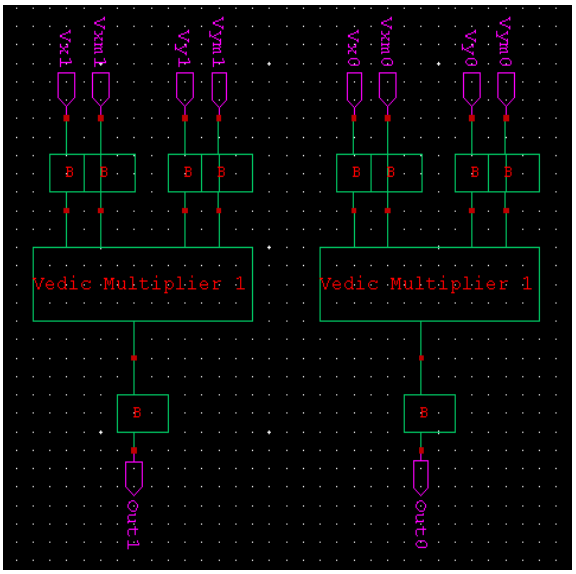


Fig 11:- 2-Sample/Bit pipeline Vedic Multiplier

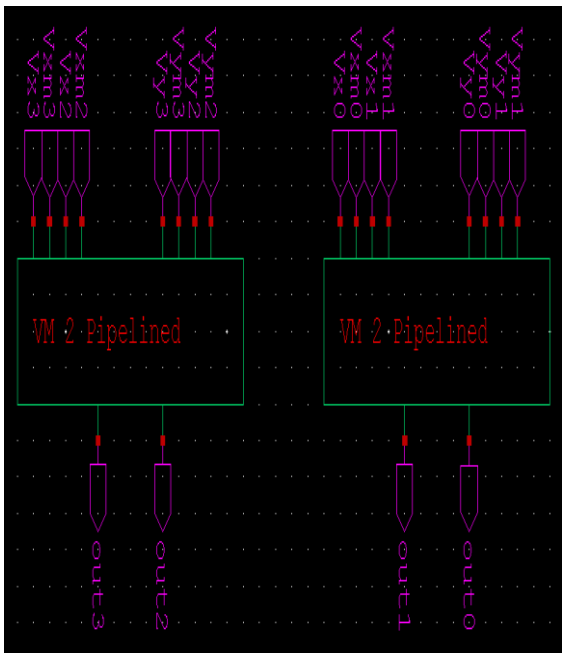


Fig 13:- 4-Sample/Bit pipeline Vedic Multiplier

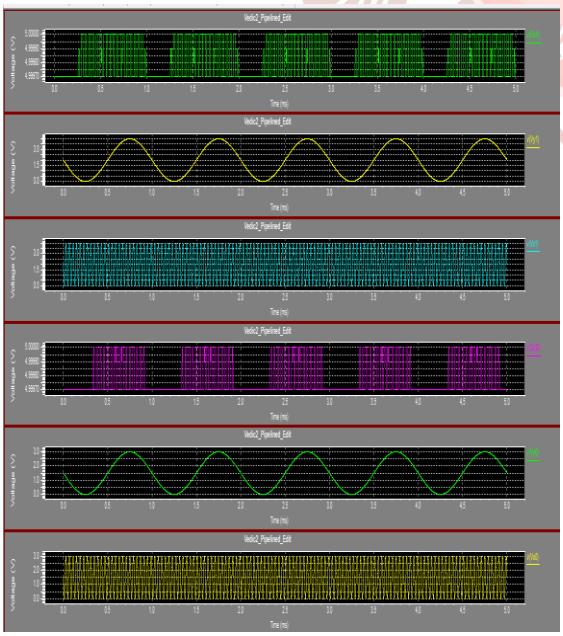


Fig. 12:-Simulation result of 2-Bit pipeline Vedic Multiplier

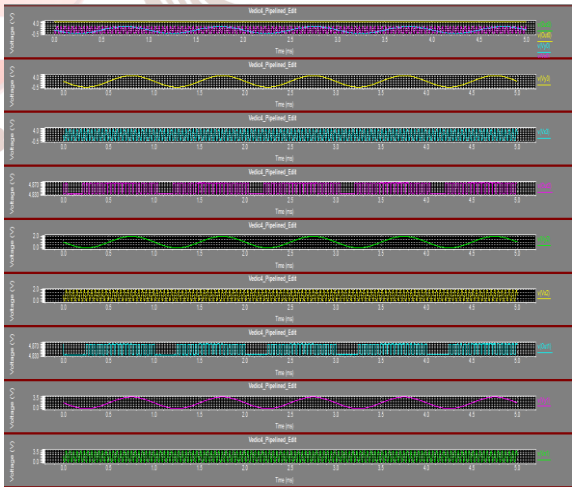


Fig. 14:-Simulation result of 4-Bit pipeline Vedic Multiplier

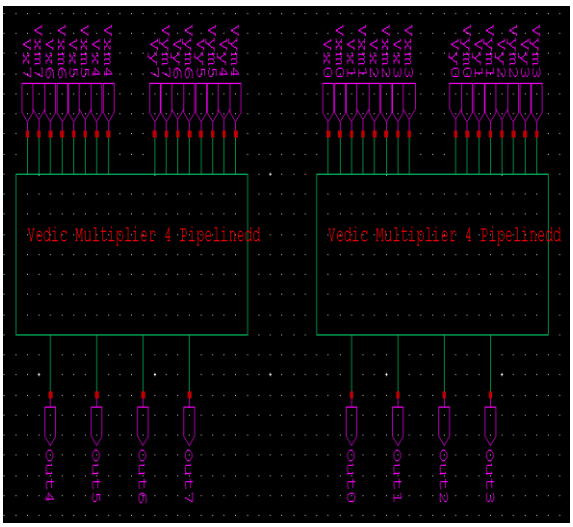


Fig 15:- 8-Sample/Bit pipeline Vedic Multiplier

Sr. no	Type of Vedic multiplier	Tech. file used	power	No. of Mossfet	Delay
1	Four quadrant multiplier	180 nm	7.2885 e-003 watt	11	13.44 u sec
	-	90 nm	4.3559 e-004 watt	11	19.85 u sec
	-	65 nm	1.8783 e-004 watt	11	21.03 u sec

Table1. Results analyses of four Quadrant Multipliers

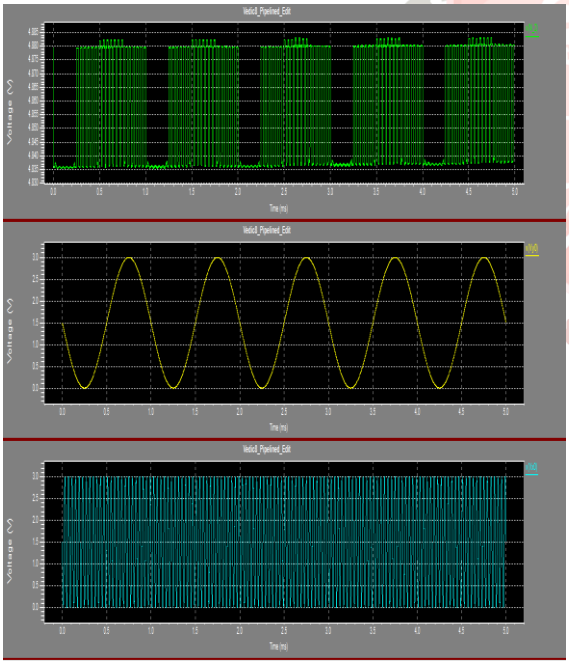


Fig. 16:-Simulation result of 8-Bit pipeline Vedic Multiplier

Table 1

Table 2

Sr. no	Type of Vedic multiplier	Tech. file used	power	No. of Mosfet	Delay
1	2 – bit multiplier	180 nm	1.7158e-002 watt	41	13.76 u sec

	-	90 nm	8.3993e-003 watt	41	18.97 u sec
	-	65 nm	8.0685e-003 watt	41	19.77 u sec
2	4 – bit multiplier	180 nm	3.4457e-002 watt	81	19.93 u sec
	-	90 nm	1.6947e-002 watt	81	19.46 u sec
	-	65 nm	1.6214e-002 watt	81	19.30 u sec
3	8 – bit multiplier	180 nm	6.8853e-002 watt	161	19.26 u sec
	-	90 nm	3.3894e-002 watt	161	18.82 u sec
	-	65 nm	3.2427e-002 watt	161	18.73 u sec

			watt		

Table2. Results analyses of different Multipliers

Table 3

Sr. no	Type of Vedic multiplier	Tech. file used	power	No. of Mosfet	Delay
1	2 – bit pip. multiplier	180 nm	3.5239e-002 watt	81	6.02 u sec
	-	90 nm	1.7618e-002 watt	81	2.56 u sec
	-	65 nm	1.5759e-002 watt	81	2.45 u sec
2	4 – bit pip. multiplier	180 nm	7.3417e-002 watt	161	5.68 u sec

	-	90 nm	2.2848e-002 watt	161	2.88 u sec
	-	65 nm	3.0772e-002 watt	161	1.76 u sec
3	8 – bit pip. multiplier	180 nm	1.4683e-001 watt	321	4.93 u sec
	-	90 nm	4.5696e-002 watt	321	4.47 u sec
	-	65 nm	6.1530e-002 watt	321	4.16 u sec

Table3. Results analyses of different pipeline Vedic Multipliers

XI. Conclusion

The paper shows the efficient use of Vedic multiplication method in order to multiply two numbers. Here we introduce the concept of pipelining so that lesser number of LUTs verifies that the hardware requirement is reduced, Thereby reducing the time consumption without compromising power so much.

X. Scope of Future Work

An improvement in power by using new techniques can greatly improve system performance. This project can be extended for the reconfigurable architecture.

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